



Osiris: Automated Discovery of Microarchitectural Side Channels

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We improve this process by fuzzing for side channels!

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int* probe_memory = malloc(4096);  
_mm_clflush(probe_memory)  
  
// potentially executed victim code  
*probe_memory;  
  
before = time();  
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after = time();  
plot(after-before);
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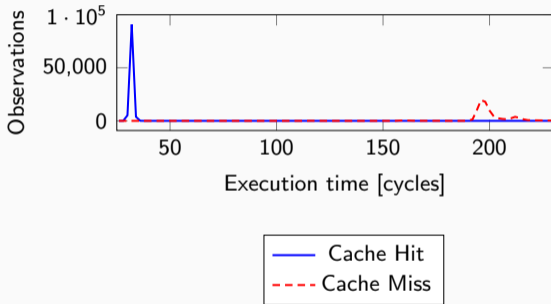
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Reset Sequence

Flush+Reload – Sequence Triple

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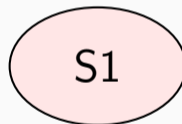
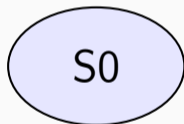
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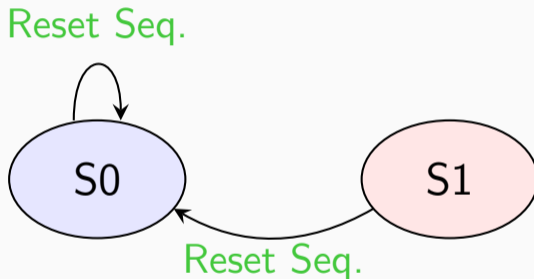
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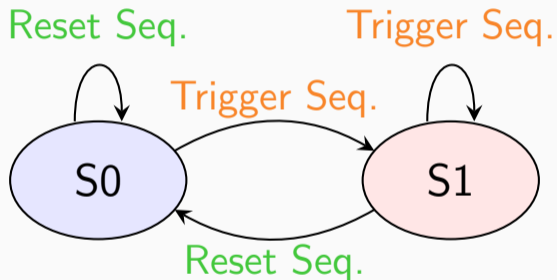
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Measurement Sequence







Testing A Sequence Triple



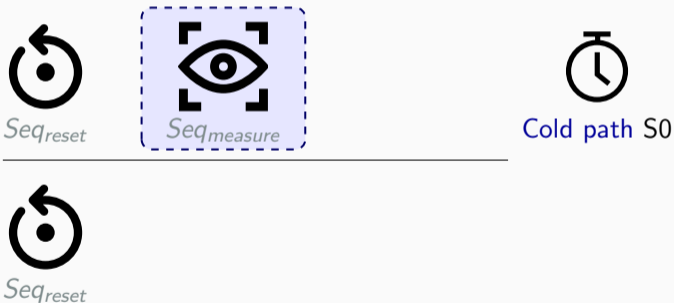
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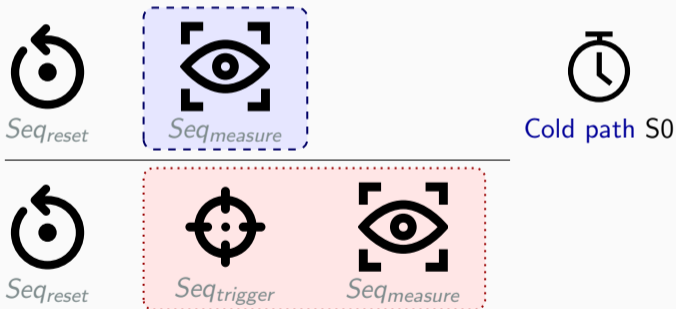
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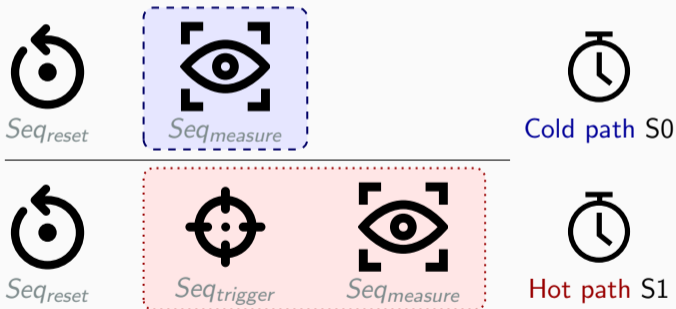
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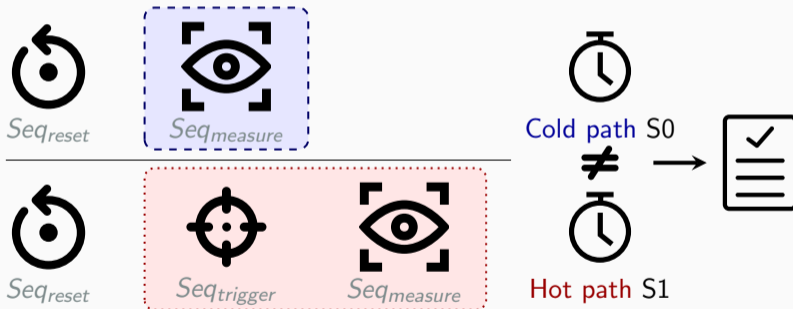
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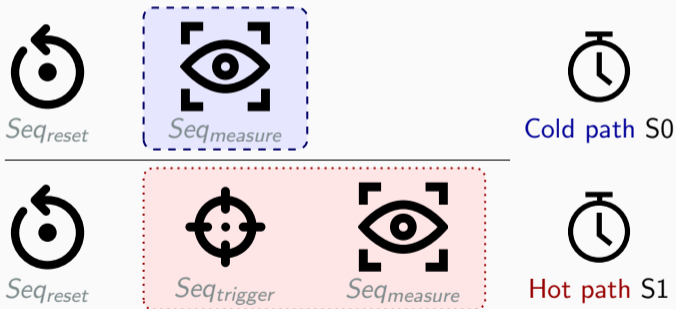


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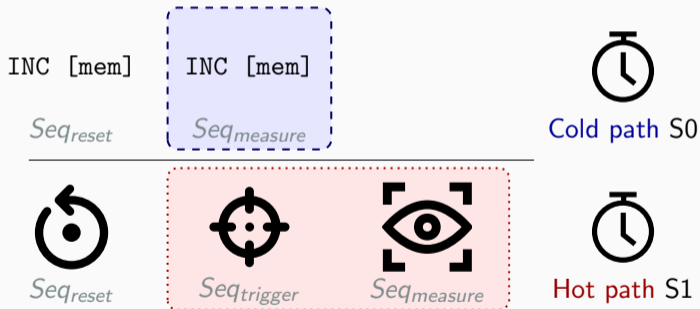
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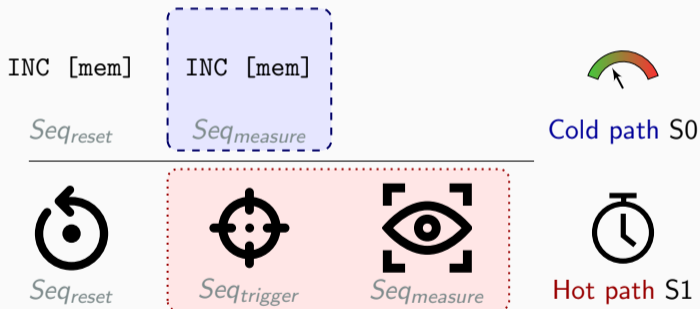
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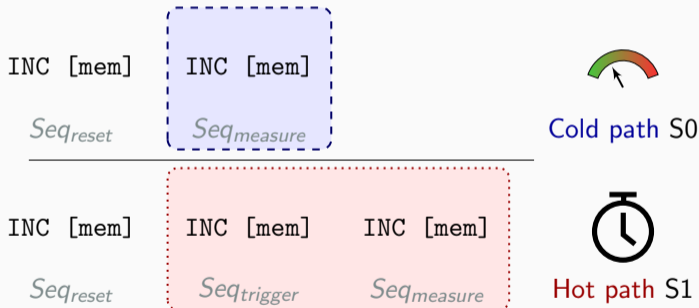
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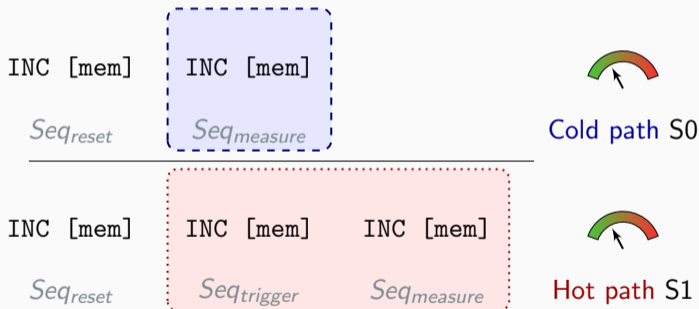
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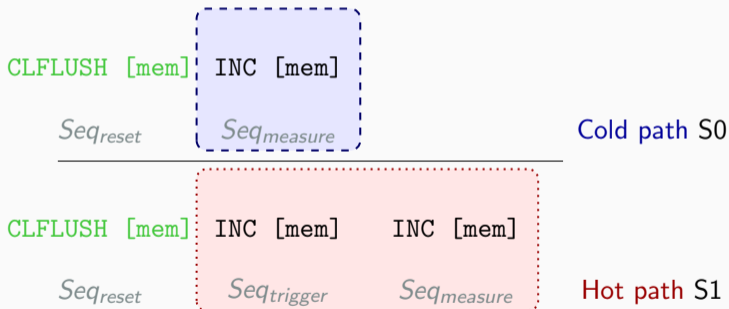
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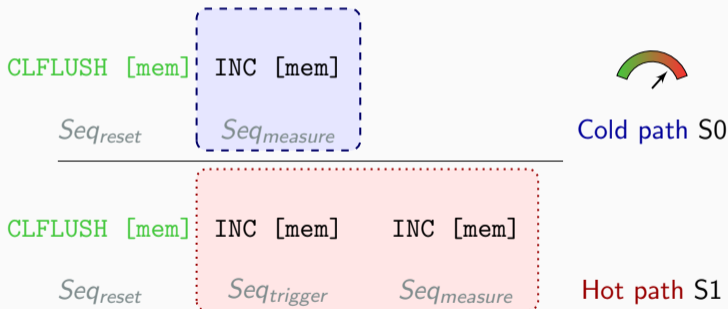
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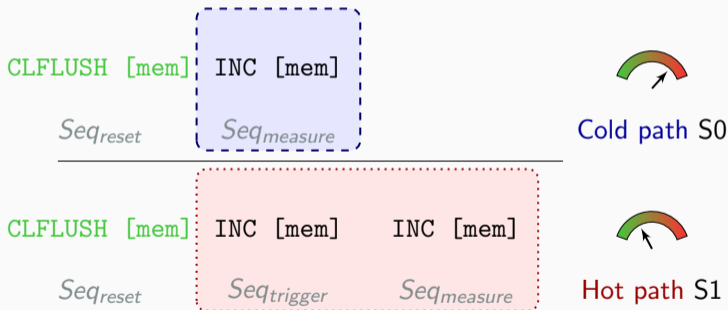
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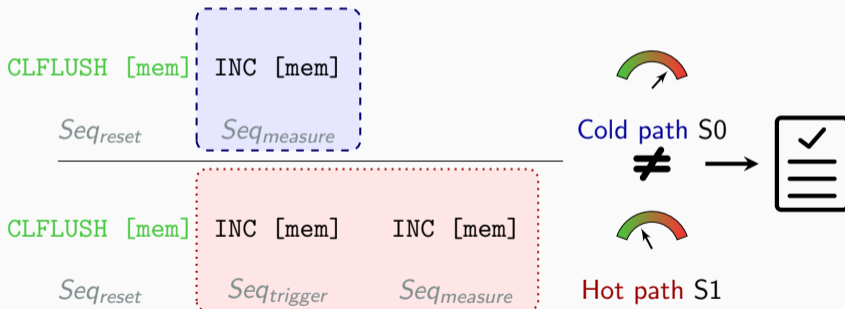
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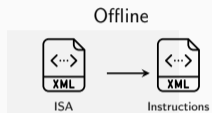
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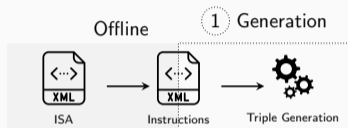


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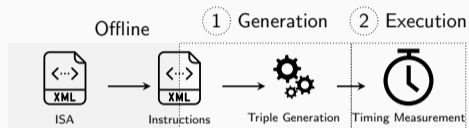
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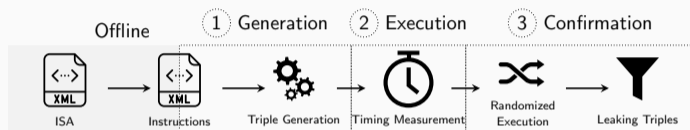




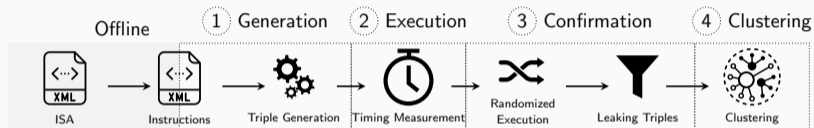
Osiris – Fuzzing x86 CPUs for Side Channels



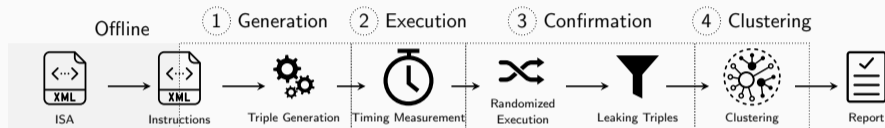
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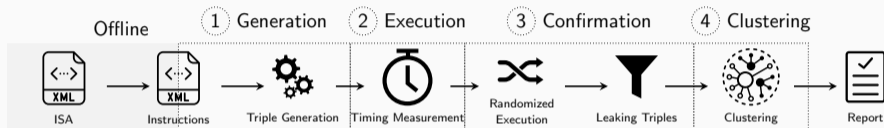


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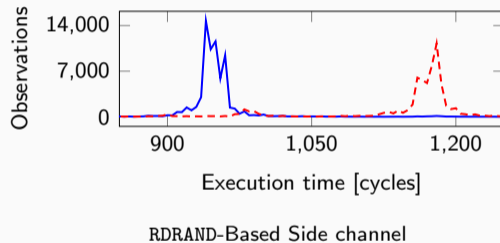
We tested Osiris on **5 different CPUs**
(AMD and Intel)

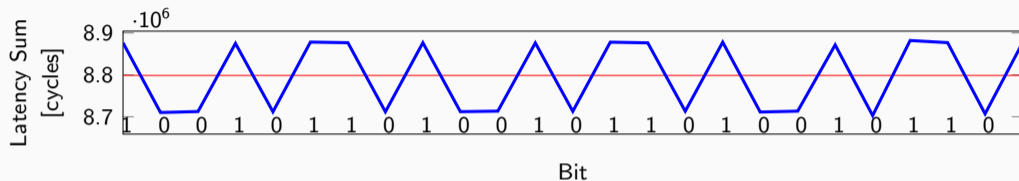
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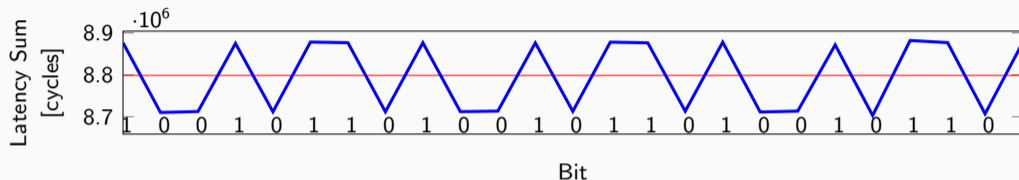
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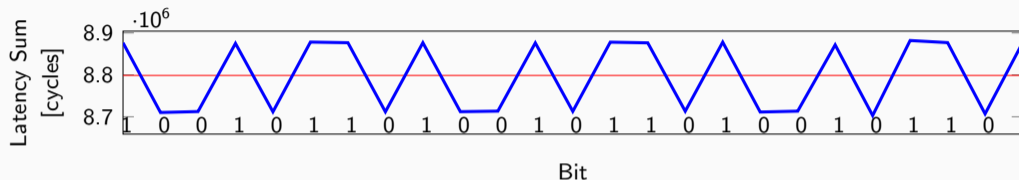




RDRAND Covert Channel Transmission on Ice-Lake



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Few requirements: no shared memory, no shared cache

Stealthy: no related performance counters

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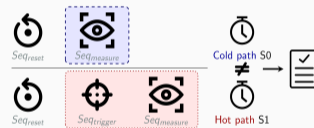
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- Works **on new Intel CPUs** (Ice Lake and Comet Lake)

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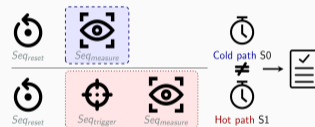
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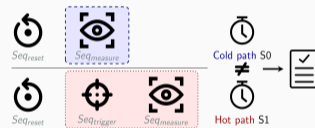
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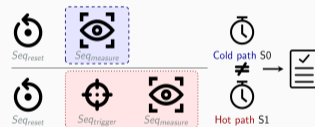
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- We found **4 novel side channels**
- We evaluated these side channels in **3 case studies**
- We **open-sourced Osiris** on <https://github.com/cispa/osiris>

