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United States

[11] 3,881,311

Hama et al.

[45] May 6, 1975

- [54] **DRIVING ARRANGEMENT FOR PASSIVE TIME INDICATING DEVICES** 3,575,492 4/1972 Nester et al. 350/160 LC
3,576,099 4/1971 Walton..... 58/50 R
3,664,118 5/1972 Walton 58/23 A
- [75] Inventors: **Tetsuro Hama; Izuhiko Nishimura,** both of Suwa, Japan 3,700,306 10/1972 Cartmell et al. 350/150

- [73] Assignee: **Kabushiki Kaisha Suwa Seikosha,** Tokyo, Japan
- [22] Filed: **Mar. 19, 1974**
- [21] Appl. No.: **452,588**

Primary Examiner—Edith Simmons Jackmon
Attorney, Agent, or Firm—Blum, Moscovitz, Friedman & Kaplan

Related U.S. Application Data

- [63] Continuation-in-part of Ser. No. 232,461, Feb. 28, 1972, Pat. No. 3,797,225.

Foreign Application Priority Data

- [30] Feb. 27, 1971 Japan..... 46-9804
- [52] U.S. Cl..... **58/50 R; 307/38; 340/336;**
350/160 LC
- [51] Int. Cl.... **G04b 19/30; H02j 3/10; H05b 39/02**
- [58] Field of Search 58/50 R; 307/38; 340/324,
340/336; 350/160 LC

References Cited

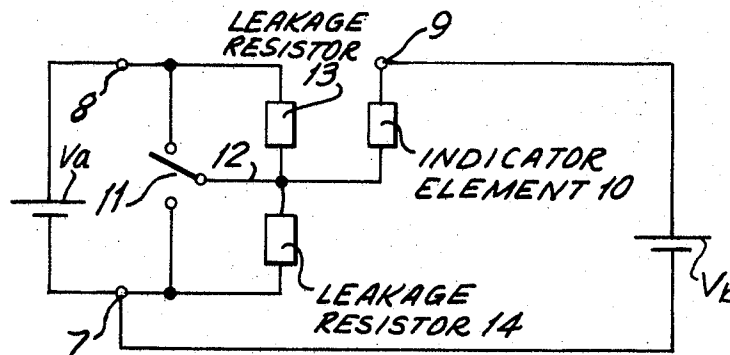
UNITED STATES PATENTS

- [56] 3,505,804 4/1970 Hotstein..... 58/50 R

[57] ABSTRACT

A driving arrangement for passive time indication devices wherein a passive indication device is connected between the output terminal of a double throw-type switching element and a terminal having a first potential such that the difference between said first potential and a second potential applied to the output terminal of said switching element when said switching element is in a first position is sufficient to excite the passive time indication device while the difference between said first potential and a third potential applied to said switching element output terminal when said switching element is in a second position is less than the threshold voltage of the passive time indication element.

9 Claims, 16 Drawing Figures



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OR IN 58/50R

FIG. 1
PRIOR ART

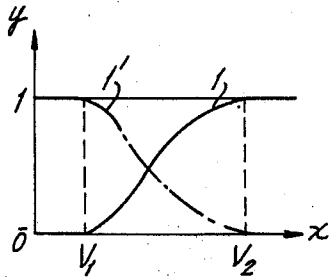


FIG. 2
PRIOR ART

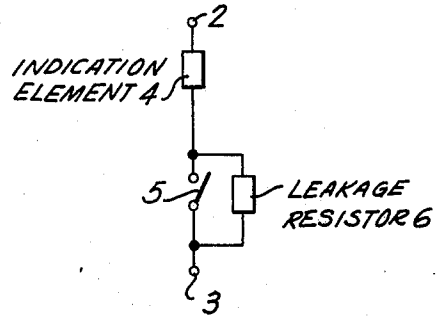


FIG. 3

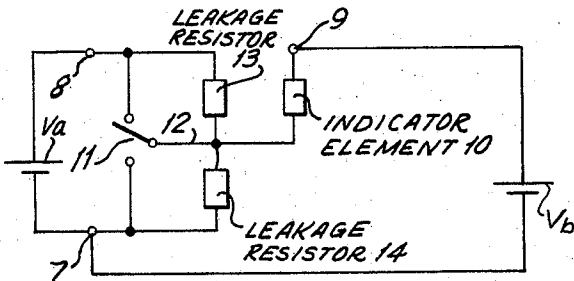


FIG. 4

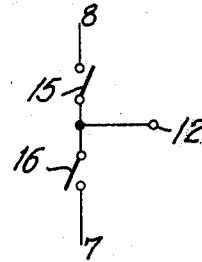


FIG. 5

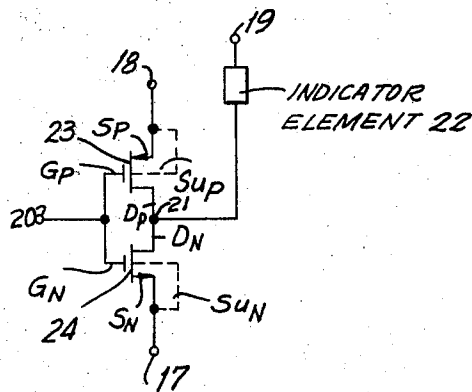


FIG. 6

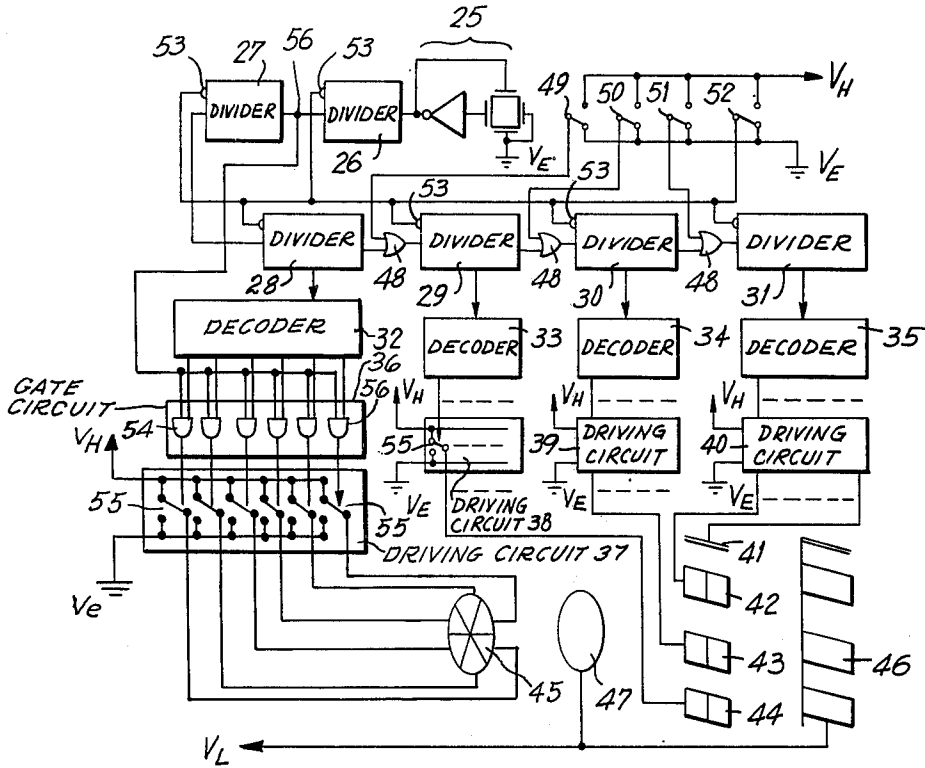


FIG. 7

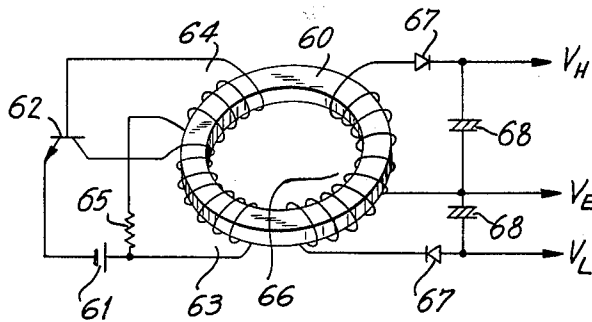


FIG. 8

STRENGTH OF THE TRANSMITTED LIGHT (ARBITRARY UNIT)

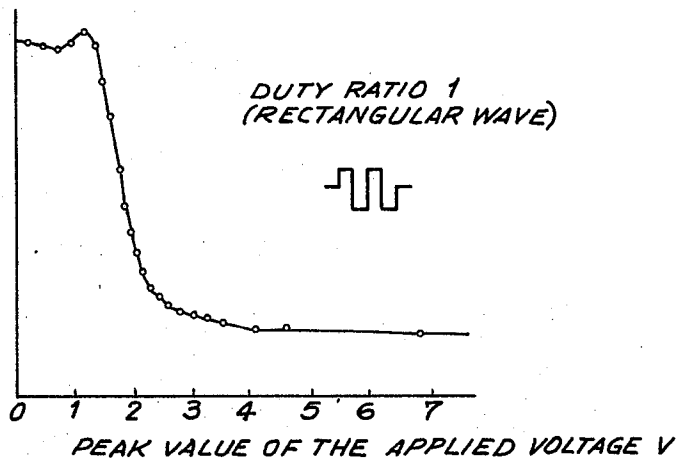


FIG. 9

STRENGTH OF THE TRANSMITTED LIGHT (ARBITRARY UNIT)

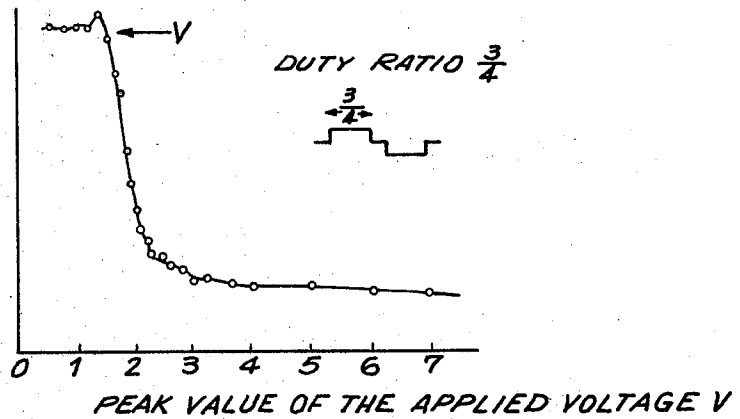
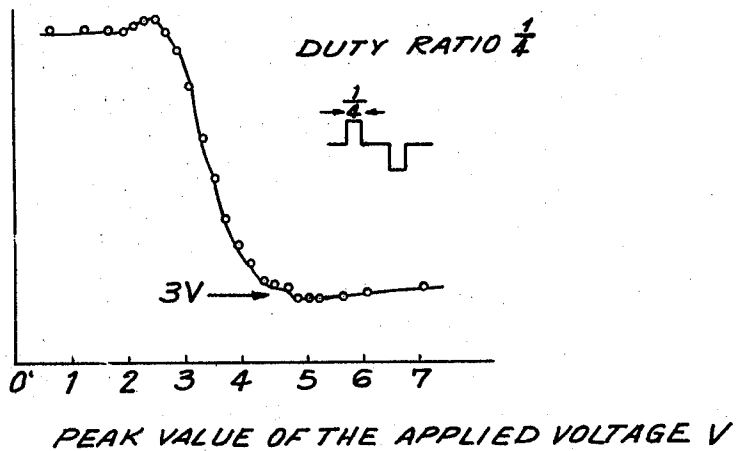


FIG. 10

STRENGTH OF THE TRANSMITTED LIGHT (ARBITRARY UNIT)



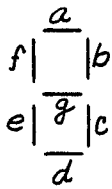


FIG. 11 a

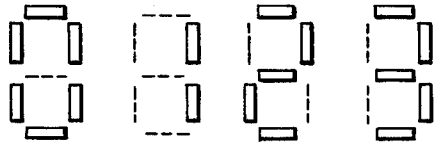


FIG. 11 b

FIG. 11 c

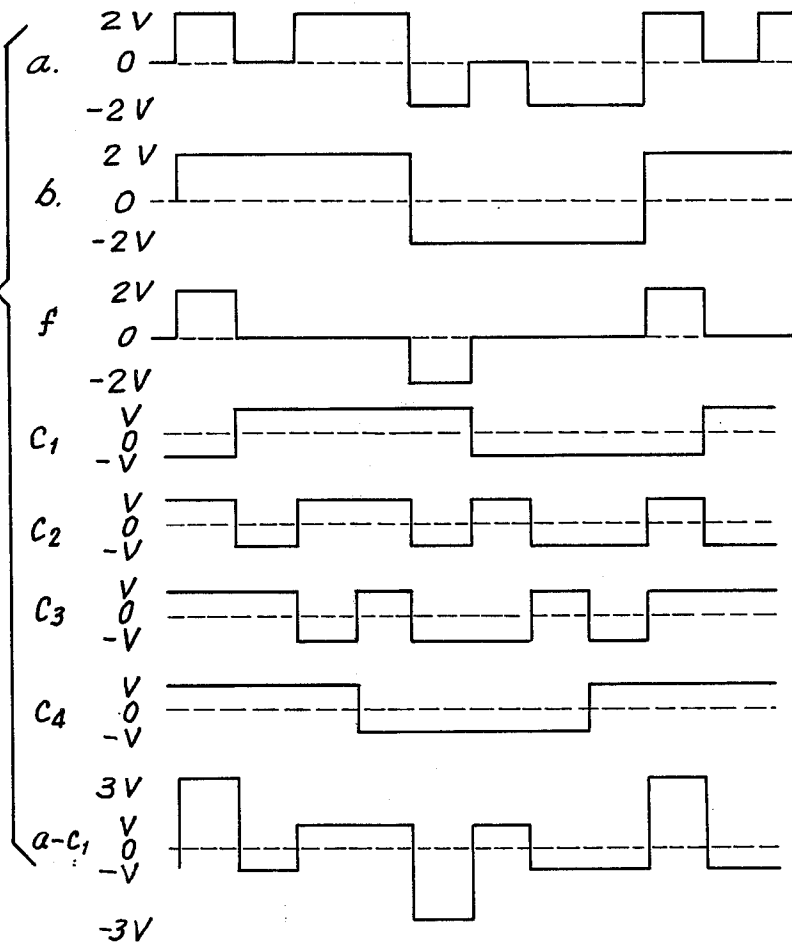


FIG. 12

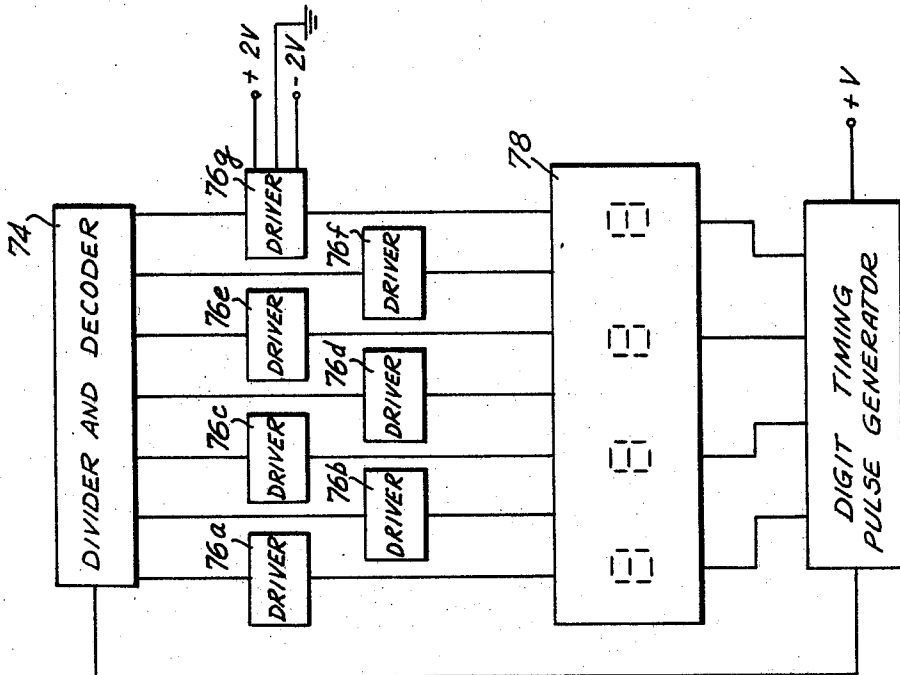


FIG. 13

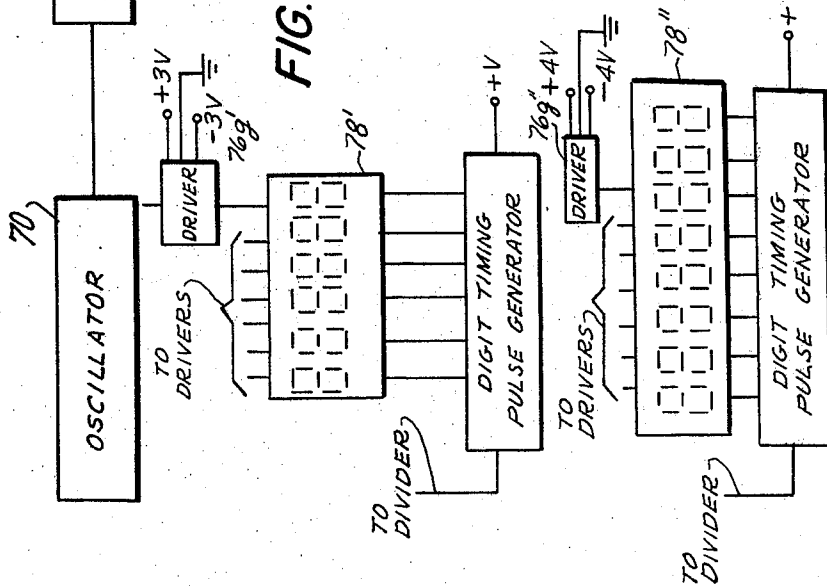
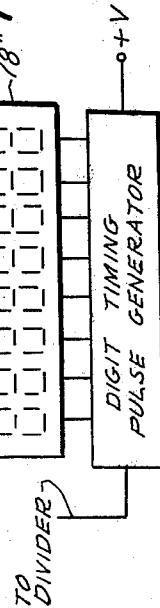


FIG. 14



DRIVING ARRANGEMENT FOR PASSIVE TIME INDICATING DEVICES

CROSS REFERENCE TO RELATED APPLICATION

This is a continuation-in-part of our co-pending application Ser. No. 232,461, filed Feb. 28, 1972 which is now U.S. Pat. No. 3,797,225.

BACKGROUND OF THE INVENTION

This invention relates to a driving arrangement for passive time indication devices adapted for actuation by an electric signal to provide a visual time indication in electric timepieces. In recent years, passive time indication elements such as liquid crystal display devices have been produced which change the condition of scattering, absorption, transmission or polarization of light in response to an electric signal in order to provide a visual display. Such passive time indication devices generally require small amounts of power for operation and are particularly suitable for application to fully electronic watches, and in particular, to small-sized fully electronic wrist watches. On the other hand, such passive indication devices generally require a high voltage for operation, resulting in the problem that a slight leakage current in the driving circuit reduces the efficiency of the indicating function. By taking into consideration the voltage characteristics of such passive time indication elements, the foregoing deficiencies have been eliminated.

SUMMARY OF THE INVENTION

Generally speaking, in accordance with the invention, a driving arrangement for passive time indication devices is provided wherein a passive time indication device is connected between the output terminal of a double throw-type switching element and a terminal having a first potential applied thereto. Said switching element may consist of a pair of separate switches connected to a common output terminal, mechanical switching devices, and solid state switching devices. Second and third potentials are respectively applied to the two inputs of said switching element for respective application to said output terminal when said switching element is one of first and second switching modes. The value of said first potential is such that the difference between said first and second potentials is sufficient for exciting said passive time indication element while the difference between said first and third potentials is less than the threshold voltage of said passive indication element.

Accordingly, it is an object of this invention to provide a driving arrangement suitable for driving passive time indication elements to provide time indication for watches.

Still other objects and advantages of the invention will in part be obvious and will in part be apparent from the specification and drawings.

The invention accordingly comprises the features of construction, combination of elements, and arrangement of parts which will be exemplified in the constructions hereinafter set forth, and the scope of the invention will be indicated in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a fuller understanding of the invention, reference is had to the following description taken in connection with the accompanying drawings, in which:

FIG. 1 is a graphical representation of the typical voltage-brightness characteristics of a passive indication element;

FIG. 2 is a block diagram of a general driving circuit for such passive indication element;

FIG. 3 is a block diagram illustrating the driving arrangement in accordance with the invention for such passive indication elements;

FIG. 4 is a circuit diagram of a second embodiment of the double throw-type switching element in accordance with the invention

FIG. 5 is a circuit diagram of one embodiment of the driving arrangement in accordance with the invention;

FIG. 6 is a block diagram of an electronic watch incorporating the driving mechanism in accordance with the invention;

FIG. 7 is a circuit diagram of a circuit for producing the three potentials required in connection with the driving arrangement in accordance with the invention;

FIGS. 8, 9 and 10 are plots of strength of transmitted light v. peak voltage of applied voltage for duty ratios of 1, $\frac{3}{4}$ and $\frac{1}{4}$ respectively;

FIGS. 11a depicts a one digit of a seven bar display, FIG. 11b depicts a four-digit digital display formed of seven-bar displays, FIG. 11c depicts selected waveform diagrams for driving the display of FIG. 11c;

FIG. 12 depicts a driving circuit for driving the display of FIG. 11b; and

FIGS. 13 and 14 respectively depict a modification of a portion of the driving circuit of FIG. 12 for the cases where the display includes six and eight digits.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to FIG. 1, a graphical representation of the voltage-brightness characteristics generally found in passive time indication elements is depicted. In said graphical representation, the axis of abscissa x represents the voltage applied to the passive time indication element with the origin being taken at \bar{O} . The axis of ordinates y represents the brightness of said passive time indication element relative to a maximum effective value for indication assigned the value of 1. Curve 1 is a voltage-brightness curve in which the brightness is low between the origin \bar{O} and a voltage V_1 , while between said voltage V_1 and a voltage V , there occurs a change from the low brightness state (not excited state) to the high brightness state (excited state).

In addition, curve 1' shows the relation between voltage and the brightness in the reverse situation to that of curve 1. The voltage V_1 is referred to as the threshold voltage in this application.

As shown in FIG. 2, when a series circuit consisting of a passive indication element 4 and a switching element 5 is inserted between voltage sources 2 and 3, and when a leakage resistance 6 present during the opened state of switching element 5 is small, the divided voltage applied to the passive indication element 4 may exceed the threshold voltage V_1 , so that said passive indication element approaches the excited state. The addition of a shunt resistance parallel to the passive indication element to compensate for the above-mentioned undesirable result is likewise undesirable, since the value of the resistance needed must be smaller than the leakage resistance 6, thereby increasing the portion of the current which is unavailable for display purposes.

The arrangement in accordance with the invention as illustrated in FIG. 3, wherein a first voltage source Va is connected between terminals 7 and 8 and a second voltage source Vb is connected between terminals 7 and 9, said second voltage source being of a value not less than said first voltage source. The input terminal of a double throw-type switching element 11 is also connected between terminals 7 and 8, said switching element having a common output terminal 12 for selective connection to either of terminals 7 and 8. A passive indication element 10 is connected between terminals 9 and 12 while leakage resistors 13 and 14 are connected between the respective input terminals 7 and 8 of double throw-type switching element 11 and passive indication element 10 (terminal 12).

As more particularly shown in FIG. 4, while a unitary double-throw switching element as depicted in FIG. 3, may be used, said double-throw type switching element may also take the form of two single-throw switching elements 15 and 16 which operate oppositely, or by any element having a similar function.

In the switching mode where terminal 12 is connected to terminal 7 through the double-throw type switching element, passive indication element 10 is connected between terminals 7 and 9, so that the voltage of the second voltage source Vb is applied thereto. On the other hand, in the switching mode wherein terminal 12 is connected to terminal 8 through said double-throw-type switching element, passive indication element 10 is connected between terminals 8 and 9, so that the difference in voltage between said first and second voltage sources Va and Vb are applied thereto. By insuring that the second voltage source Vb is of a value great enough to excite passive indication element 10, and by insuring that the voltage of the first voltage source Va is of a value less than the value of said voltage of said second voltage source Vb by an amount within the range wherein said passive indication element will not be excited (i.e., a value less than the threshold voltage), the excitation condition of the passive indication element can be regulated by setting the switching mode of double throw-type switching element 11 between two values.

By selecting the first voltage source so that it has a value less than the second voltage source, it is possible to use semiconductor switching elements having non-linear leakage resistance in response to voltage as the double throw-type switching element. An example of such an arrangement is depicted in FIG. 5, wherein the double throw-type switching element consists of an enhancement type P-channel insulated gate field effect transistor 23 and an enhancement type N-channel insulated gate field effect transistor 24. The passive indication element 22 is in the form of a nematic liquid crystal. Taking the potential at a terminal 17 connected to the source of transistor 24, a first positive potential is applied to terminal 18 connected to the source of transistor 23 and a second positive potential sufficient to excite indication element 22 and a value not less than the value of said first positive potential is connected to terminal 19, which in turn is connected to one side of passive indicator element 22, the other side of said passive indicator element being connected to common output terminal 21 connected between the respective drains of transistors 23 and 24. The difference between the second positive potential and the first positive po-

tential is selected to be smaller than the threshold voltage of passive indication element 22.

The control of the double throw-type switching element of FIG. 5 is achieved through terminal 20 connected to the respective gates of transistors 23 and 24. Thus, said transistors are placed in a first switching mode when a potential nearly equal to the potential of terminal 17 (approximately zero potential) is applied to terminal 20. In this mode, gate G_N of transistor 24 is placed at nearly zero potential so that the resistance between the source S_N and the drain D_N thereof is placed at an extremely large value. On the other hand, the gate G_P of transistor 23 is given a potential of one direction so that the resistance between source S_P and drain D_P decreases substantially. As a consequence, the potential at the common connecting electrode 21 between the respective drains of transistors 23 and 24 becomes equal to the first positive potential applied to terminal 18 and a voltage nearly equal to the difference between the second and first positive potential is applied to passive indication element 22. Since this difference potential is lower than the threshold voltage of said passive indication element, said element is not excited. At this time, if the current flowing from terminal 19 to terminal 21 exceeds the current flowing from drain D_N of transistor 24 to terminal 17, drain D_P of transistor 23 assumes a positive potential relative to terminal 18. However, since a diode has been formed in one direction between drain D_P of transistor 23 and the substrate Su_P thereof, the potential in question becomes almost equal to the potential of terminal 18.

In the second switching mode, wherein a positive potential nearly equal to the potential of terminal 18 is applied to terminal 20, gate G_P of transistor 23 is placed at nearly zero potential so that the resistance between source S_P and drain D_P thereof are brought to an extremely large value. On the other hand, the gate G_N of transistor 24 has a potential of one direction applied thereto so that the resistance between source S_N and drain D_N thereof is reduced considerably. For this reason, the potential at common connecting terminal 21 is substantially at the standard potential (zero potential) and a potential nearly equal to the second positive potential is applied to passive indication element 22 to excite said element.

While in the foregoing embodiment, a pair of transistors was incorporated as the double throw-type switching element, other suitable double throw-type switching elements may be substituted therefor consisting either of unitary switching elements or combinations of switching elements, provided the functions of the double throw-type switching elements of FIGS. 3 and 4 are performed.

Referring now to FIG. 6, a block diagram of a watch incorporating the driving arrangement in accordance with the invention is depicted. In said embodiment, the double throw-type switching element 55 may take the form of a complementary insulated gate field effect transistor arrangement such as is depicted in FIG. 5. Further, the passive indication elements are of the nematic liquid crystal type, the indication elements providing a digital display of hours and minutes through the use of a seven bar display capable of displaying any number from 0 to 9 at each digit of said hour and minute indication. For this purpose, each digit would be represented by a liquid crystal display device of the passive indication type having a common electrode, a

segmented electrode formed from said seven bars and liquid crystal material of the nematic type therebetween. Indication of seconds is formed by means of a round liquid crystal display having six pie-shaped sectors which are sequentially flickered in response to a signal having a period of one second, each of the pie-shaped sectors being flickered for a period of 10-seconds.

In the electronic watch of FIG. 6, a high frequency time standard signal is generated in an oscillator 25 and divided into a signal having a 1-second period by a frequency divider 26. The 1-second signal from divider 26 is applied to a 1/10 divider 27 which serves to count the 1-second signals to produce a 10-second signal for application to 1/6 divider 28. Divider 28 counts the 10-second signals to produce a 1-minute signal for application to the next stage.

The state output of 1/6 counter 28 is applied to a decoder 32 adapted to produce six output signals, one of said output signals being associated with each of the sectors of the second indicator. Said output signals are applied to gate circuits 36 which consist of six AND gates 54, one of which is associated with each second indicator sector, for receiving the associated output signal from decoder 32 and a 1-second signal from terminal 56 connected to the output of divider 26. The output of each AND gate 54 is connected to the control of a double throw-type switching element 55, in this case to the respective gates of the insulated gate type field effect transistors, to control the switching mode of said switching element. The input terminals of each switching element 55 in driving circuit 37 are respectively connected to ground potential V_E and to potential V_H . The output terminal of each of said switching elements is connected to one of the sector electrodes 45 of the second indicator, the common electrode 47 thereof being connected to voltage V_L . In this manner, each sector is sequentially flickered at a frequency of one Hz for a period of 10 seconds.

A 1/10 divider 29 receives the 1-minute signal from divider 28 through OR gate 48, and produces a 10-second signal output. The state output of divider 29 is applied to a decoder 33 for producing seven outputs corresponding to the seven bars on the minute digit display segmented electrode 44. Each output of decoder 33 is applied to a double throw-type switching element 55 in driving circuit 38 which functions in a manner similar to the double throw-type switching element 55 of driving circuit 37. In a similar manner, divider 30 receives the 10-minute signal from divider 29 through OR gate 48 to produce a 1-hour signal. The state signals of divider 30 are applied to decoder 34 to driving circuit 39 which provides the driving voltages for the seven bar display of the 10-second digit represented by segmented electrode 43.

Finally, the 1-hour signal output of 1/6 divider 30 is applied to a 1/12 divider 31, the state of which drives the 10-hour digit segmented electrode 42 through decoder 35 and driving circuit 40 in the same manner as the other digits of the display. A switch 52 resets the states of the respective frequency dividers and counters to their initial states through a connection to terminals 53 thereof, while switches 49, 50 and 51 set the respective digits of the 1-minute display the 10-minute display and the 1-hour display to the desired figures by connection to the respective OR gates 48. Each time one of switches 49, 50 and 51 is in its respective ON state, a

digit is added logically to the divider associated therewith so as to add one count to each divider to advance the state of that divider by one digit.

In the embodiment of FIG. 6, the potentials of the respective segmented electrodes are selectively alternated between values substantially equal to V_H or V_E by corresponding double throw switching elements in correspondence with the time to be indicated, while common electrodes 46 and 47 of the passive display elements are maintained at a potential V_L . Accordingly, the potential difference between each segment of the respective segmented electrodes 41, 42, 43, 44 and 45 is:

$$V_C = V_H - V_L,$$

or

$$V'_C = V_E - V_L.$$

When a nematic phase liquid crystal is driven, it is necessary that, taking the threshold voltage as V_{TH} and the voltage sufficient for indication as V_{ON} , that said potential should conform to the following relations:

$$V_C < V_{ON},$$

and

$$V'_C < V_{TH}.$$

Since,

$$V_C < V_H - V_E,$$

it is possible in the arrangement in accordance with the invention to supply a voltage higher than the voltage applied to the driving circuit to the indication element as mentioned above, so that substantial advantages such as clear visibility of indication, simplification of design of driving circuit and reduction of electric power consumption can be achieved.

Referring now to FIG. 7, one example of a voltage boosting circuit for obtaining potentials V_H , V_E and V_L from a single battery is depicted. In such circuit, a toroidal core 60 which provides maximum boosting efficiency while minimizing size is wound with a driving coil 63 and a detecting coil 64. Driving coil 63 is connected across the series connection of a battery 61 and the emitter-collector path of a transistor 62. Driving coil 64 is connected between a resistor 65 and the base of said transistor. An oscillating AC voltage is delivered to the secondary coil 66 and is rectified by diodes 67 and smoothing condensers 68 to produce the desired potentials V_H , V_E and V_L , which satisfy the conditions required in accordance with the invention.

FIGS. 8 - 12 are directed to an embodiment of a watch wherein a liquid crystal display device is dynamically driven. Such dynamic driving is particularly appropriate for use with twist-type liquid crystal displays utilizing liquid crystals having positive dielectric anisotropy operated in the field effect mode. Such liquid crystals and their optical activity are described in Schadt and Helfrich, Voltage-dependent Optical Activity Of A Twisted Nematic Liquid Crystal, 18 Applied Physics Letters 127-28 (Feb. 15, 1971). The twisted orientation of the liquid crystal material is created by rubbing the inner surface of one of the plates of liquid crystal display in a first direction and rubbing the inner surface of the other plate of the liquid crystal display in a direction oriented 90° to said first direction. Crossed polarizers are provided, one on each side of

the liquid crystal display and oriented, in one application, so that each polarizer is oriented in the same direction as the direction of rubbing of the adjacent plate. When a voltage is applied between electrodes deposited on the plate above a threshold voltage, light which normally is transmitted through the liquid crystal display is cut off.

FIG. 8 represents a plot of the strength of transmitted light through the liquid crystal device in arbitrary units vs peak value of the applied voltage. The applied voltage is in the form of rectangular AC pulses. The reduction in the strength of the transmitted light with the increase in voltage, i.e., the changing of the state of the display from one of light to darkness or light transmission to light blocking, is depicted. The liquid crystal cell is characterized by a clearing threshold of voltage between one and three volts, the phenomenon being saturated at several volts.

FIGS. 8 and 9 show a similar plot of strength of transmitted light vs peak value of the applied voltage where the duty ratio of the applied voltage is $\frac{3}{4}$ and $\frac{1}{4}$ respectively. A comparison of FIGS. 8 and 9 reveals that, in the case of a duty ratio of $\frac{3}{4}$, the threshold voltage and saturation voltage are substantially unchanged as compared with the case where the duty ratio is 1 (FIG. 8). However, in the case of a duty ratio of $\frac{1}{4}$, the threshold and saturation voltages are shifted horizontally in the high voltage direction. Specifically, the smaller the duty ratio becomes the higher the saturation voltage.

Referring to FIG. 11a, a typical seven-bar display orientation is depicted with each of the bars assigned a letter. In FIG. 11b, a four digit display, such as might be included in an electronic timepiece, is depicted. Each of the digits are represented by a seven-bar display, the four digits respectively displaying the numbers 0, 1, 2 and 3. FIG. 11c depicts a series of driving waveforms for the four digit display of FIG. 11b wherein said display is dynamically driven. A circuit for dynamically driving the display of FIG. 11b is depicted in FIG. 12. The electronic timepiece depicted includes an oscillator 70 for producing a high frequency time standard signal which is applied to divider circuit 72 which produces an intermediate frequency signal from the high frequency time standard signal of oscillator 70. The intermediate frequency signal 72 is applied to further divider and decoder circuits 74 which produce the time keeping signals in accordance with the invention. The four-digit liquid crystal display 78 is provided with electrodes defining seven-bar displays for each digit on one plate of the liquid crystal cell. All of the *a* bar (FIG. 11a) electrodes are electrically connected together as are all of the *b*, *c*, . . . , *g* bars respectively so that there are seven output terminals on the plate of the liquid crystal cell bearing the seven-bar segments. Separate common electrodes are provided for each digit on the other plate of the liquid crystal cell so that there are four output terminals on the other plate, one associated with each digit. The output of divider and decoder circuit 74 is applied to seven driver circuits 76a, 76b, . . . , 76g, each of which is connected to the correspondingly lettered bar of the seven-bar displays. Each of the driver circuits includes double throw-type switching elements such as are depicted in driving circuit 37 of FIG. 6, the input voltages applied to each driver being $\pm 2V$ and ground. The intermediate frequency signal from divider circuit 72 is also applied to a digit timing pulse generator 80 which applies timing pulses to the

common electrodes of the four digits of the liquid crystal display 78. These pulses are of t voltage $\pm V$ as will be seen in connection with the waveforms of FIG. 11c.

In FIG. 11c, the output of the drivers 76a, 76b and 76f are depicted at waveforms *a*, *b* and *f* respectively. These are the waveforms required to display the numbers shown in FIG. 11b. The timing pulses applied to the respective common electrodes are depicted in waveforms *c*₁, *c*₂, *c*₃ and *c*₄. The net voltage applied to the *a* bar of the first digit during each cycle is depicted in the waveform *a-c*₁ of FIG. 11c.

Applying waveform *a-c*₁ to FIGS. 8 and 9, we find that upon the application of the first pulse, which is of a magnitude of 3V and a duty ratio of $\frac{1}{4}$, the display panel is saturated and becomes dark as shown in FIG. 9.

The next pulse has a peak value of $-V$ and a duty ratio of $\frac{1}{4}$ while the next pulse has a peak value of V and a duty ratio of $\frac{1}{2}$. Both of these voltages are less than the threshold voltage as shown by FIGS. 8 and 9 so that the display panel becomes light although the circuit is in the OFF state. If absolute value alone is considered, the latter pulse may be regarded as a pulse having a peak value of V and a duty ratio of $\frac{3}{4}$, and accordingly, is clearly less than the threshold voltage. The alternating pulse is repeated each half period whereby each of the digits are actuated during each period using a time-division dynamic driving method.

It is apparent from the foregoing that it is preferable in the driving method in accordance with the invention to apply to one of the electrodes, either the common or the segmented electrodes, a voltage less than the threshold voltage V_{th} and a voltage to the other of the electrodes such that the net voltage across the liquid crystal cell when it is to be rendered visible is larger than the threshold voltage. Thus, in the case of four digits to be dynamically driven, where the voltage is less than the threshold voltage is V , a net voltage of 3V may be provided between the electrodes by proper application of the voltage to the other electrodes. Similarly, where 6 or 8 digits are to be dynamically driven, so that the duty ratio is $\frac{1}{6}$ or $\frac{1}{8}$, the voltage applied to one of the sets of electrodes would be V , and the net voltage applied between the electrode would be 4V and 5V respectively. Thus, as shown in FIG. 13, where six digits are provided in liquid crystal display 78', the digit timing pulse generator is adapted to produce six timing pulses and each driver 76' is energized by $\pm 3V$. As shown in FIG. 14, when eight digits are provided in liquid crystal display 78'', the digit time impulse generator is provided with eight outputs and each driver 76'' is energized with $\pm 4V$.

The foregoing dynamic driving approach improves the reliability of the circuit and reduces the number of elements by reducing the number of leads. This results in a substantially reduced manufacturing cost.

It should be noted that with the decrease in the duty ratio, the peak value required for producing the same brightness increases. This results from the fact that the pulse width applied to each segment per digit decreases as the number of digits for display increases. Accordingly, the peak value of the applied pulse voltage must be increased as the duty ratio decreases. A display cell having the same brightness can be obtained by roughly estimating the effective value which is the means

square of the applied electric power and applying the voltage of that value.

It will thus be seen that the objects set forth above, and those made apparent from the preceding description, are efficiently attained and, since certain changes may be made in the above construction without departing from the spirit and scope of the invention, it is intended that all matter contained in the above description or shown in the accompanying drawings shall be interpreted as illustrative and not in a limiting sense.

It is also to be understood that the following claims are intended to cover all of the generic and specific features of the invention herein described, and all statements of the scope of the invention which, as a matter of language, might be said to fall therebetween.

What is claimed is:

1. An electronic timepiece comprising oscillator means for producing a high frequency time standard signal; divider circuit means for producing an intermediate frequency signal and low frequency timing signals in response to said high frequency time standard signal; decoder means for producing display actuation signals in response to said timing signals; driving circuit means coupled to said decoder means and including double throw-type switching means connected for selective disposition in one of first and second switching modes in response to display actuation signals; liquid crystal display means defining passive indication means and including at least four digits for the visual indication of time, each of said digits of said display including seven segmented electrodes oriented in a seven-bar display and a common electrode, corresponding segments of said segmented electrodes being electrically connected together, one of said driving circuit means being connected to each of said commonly connected segments; and digit timing pulse generator means respectively connected to each of said common electrodes for sequentially applying said first potential to each of said common electrodes, said double throw type switching means having first and second input terminals and an output terminal for selective placement in either of said first switching mode at which said first input and said output terminals are coupled and said second switching mode at which said second input and said output terminals are coupled, each said switching means output terminal being connected to one group of corresponding segmented electrodes; and means for applying a second and third potentials to said first and second switching means input terminals, respectively, said potentials being selected to have a value such that the difference between said first and second potentials is sufficient to actuate said passive indication means to provide a visual indication, and the difference between said first and third potentials is less than the threshold voltage of said passive indication means at which such visual indication is first produced.

2. A driving arrangement as recited in claim 1, wherein said double throw-type switching means includes a pair of coordinately actuated single throw-type switching means, one of said single throw-type switching means being connected between each of said inputs and said output.

3. A driving arrangement as recited in claim 1, wherein said double throw-type switching means comprises an N-channel and a P-channel field effect transistor connected with their respective source-drain paths in series, the respective gates being connected together

for coordinate actuation, said output being at the intersection of the respective source-drain paths, said inputs being on the side of said source-drain paths, said inputs being on the side of said source-drain paths opposite from said output.

4. An electronic timepiece as recited in claim 1, wherein said liquid crystal material is characterized by positive dielectric anisotropy.

5. An electronic timepiece comprising oscillator means for producing a high frequency time standard signal; divider circuit means for producing low frequency timing signals in response to said high frequency time standard signal; decoder means for producing display actuation signals in response to said timing signals; driving circuit means coupled to said decoder means and including double throw-type switching means having first and second input terminals and an output terminal for selective placement in either of a first switching mode at which said first input and said output terminals are coupled and a second switching mode at which said second input and said output terminals are coupled, said double throw-type switching means being selectively disposed in one of said first and second switching modes in response to said display actuation signals; liquid crystal display means having at least four digits of display, each of said digits including seven segmented electrodes oriented in a seven-bar display and a common electrode, corresponding segmented electrodes of each digit being electrically connected together and being connected to one of said driving circuit means for receiving the voltage from the output terminal of the double throw-type switching means thereof; and digit timing pulse generator means connected to each of said common electrodes of said liquid crystal display means for sequentially applying a first potential thereto during assigned portions of the cycle of operation thereof; and means for applying a second and third potential to said first and second switching means input terminals respectively, said potential being selected to have a value such that the net difference between said first and second potentials is sufficient to actuate said liquid crystal display means to provide a visual indication at the segmented electrodes associated with the liquid crystal material across which said net potential difference appears, and the net difference between said first and third potentials is less than the threshold voltage of said liquid crystal material at the duty cycle of said digit timing pulse generator means at which such visual indication is produced.

6. An electronic timepiece as recited in claim 5, wherein said liquid crystal material is of positive dielectric anisotropy and said liquid crystal display is of the twist-type.

7. An electronic timepiece as recited in claim 5, including four digits of display, said digit timing pulse generator means having a duty cycle of $\frac{1}{4}$, said second potential being of a voltage V less than the threshold voltage of said liquid crystal material at said $\frac{1}{4}$ duty cycle, the net potential difference between said first and second potentials being about $3V$.

8. An electronic timepiece as recited in claim 5, wherein said liquid crystal display means includes six digits, said digit timing pulse generator having a duty cycle of $\frac{1}{6}$, said first potential having a value of V less than the threshold voltage of said liquid crystal material at said duty cycle, said net potential difference between said first and second voltages being equal to about $4V$.

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9. An electronic timepiece as recited in claim 5, wherein said liquid crystal display means includes eight digits, said digit timing pulse generator means having a duty cycle of $\frac{1}{6}$, said first potential having a value V less than the threshold voltage of said liquid crystal ma-

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terial at said duty cycle, the net potential difference between said first and second potentials being equal to about 5V.

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