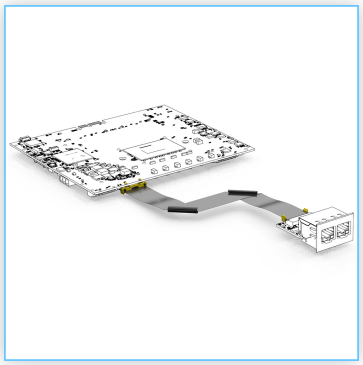
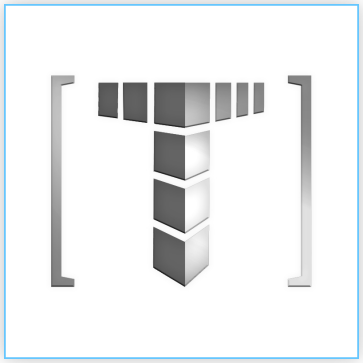
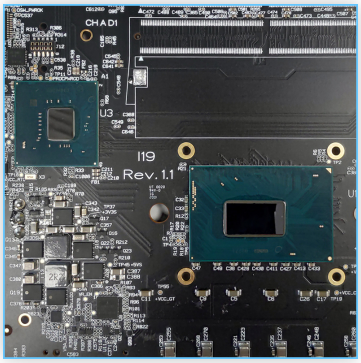
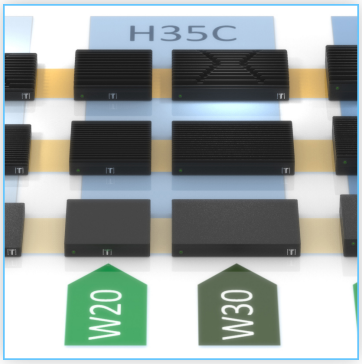


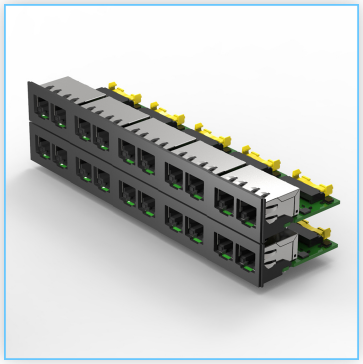
Compulab

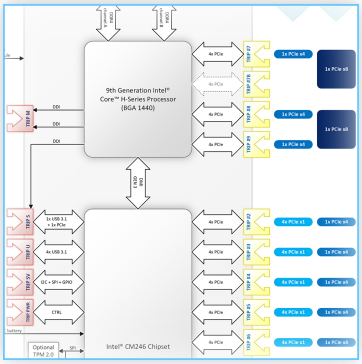
Introduction to Tensor PC











Revision 1.0
30-Apr-2020

Executive summary

- Tensor-PC is a new IIOT fanless mini-PC supporting multiple modules with mix-and-match
- Enclosure of Tensor-PC is parametric with independent choice of width, height and cooling ribs
- These design features allow the buyer of Tensor PC to choose the types and amounts of:
  - Storage devices
  - Power input
  - I/O ports
  - Networking ports
  - Extensions
- Tensor-PC offers dozens of different modules to choose from. Additional modules are developed in a progressive manner
- Modules are open-source-hardware in order to provide a reference to 3rd parties developing custom modules
- Tensor-PC supports multiple off-the-shelf cards in PCIe, mini-PCIe and M.2 form factors
- The first Tensor-PC model - [I20A] - is based on Intel 9th generation Core / Xeon with up to 6 cores, 64 GB RAM and 37 lanes of PCIe
- Tensor-PC is introducing a new industrial-temperature predictable-performance rating with no-throttling
- Tensor-PC supports out-of-band management as well as identification and control of connected modules

About Tensor-PC

Tensor-PC is a new mini-PC design by Compulab, intended to address diverse requirements in the IIOT market.

The design concept of Tensor-PC is different from previous generations of Compulab mini-PCs, introducing high-granularity modular design and a parametric enclosure. Compulab engineering team has been working for two years on the definition and implementation of this design concept.

About this document

This document explains the key features of Tensor-PC and the benefits we believe these features bring to IIOT projects. It focuses on Tensor-PC I20A ("[I20A]") which is the first Tensor-PC model we introduce.

Along the document [I20A] is often compared to previous generations of Compulab mini-PCs like IPC family and fitlet family in order to underline the changes in design.

The document contains many Tensor-PC-specific terms like "TRIP", "TEL", "TPU" etc. For your convenience, glossary can be found at the end of the document.

What "Tensor-PC" stands for

A Tensor is a mathematical object described as an array of composite elements.

A key property of Tensor-PC is that storage, power, I/O, networking and extensions ("SPINE") are each implemented as a "Tensor Element" ("TEL"). Each Tensor-PC is built by mixing and matching TELs. Therefore, naming Tensor-PC after the mathematical Tensor may be apt.

Tensor-PC naming convention

Tensor-PC I20A is the first Tensor-PC model Compulab is introducing.

"I20A" stands for:

- I: Based on an Intel CPU
- 20: Introduced in 2020
- A: model A

We use the notation [I20A] as an abbreviation of Tensor-PC I20A.

This convention allows consistent naming of future Tensor-PC models. For example, if in 2023 Compulab introduces two different AMD-based Tensor-PC models, they will be named Tensor-PC A23A ("[A23A]") and Tensor-PC A23B ("[A23B]").

How (I20A) fits in Compulab product line

Compulab is looking to offer at least one platform in each of the following power and performance categories:

Category 1: Up to 10W

Miniature, low-cost computers.

Current Compulab offering is fitlet2.

Category 2: Up to 30W

Small and modular low-power computers usually based on embedded derivatives of mobile CPUs.

Compulab offering until 2019 is IPC2/3, replaced by [I20A] in 2020.

Category 3: Up to 60W

High-performance industrial-grade computers that are compact and modular.

Compulab offering in category 3 is yet to be announced.

Category 4: 100W+

Ruggedized workstation/server for demanding applications in harsh environments.

Current Compulab offering is Airtop3.

Note: [I20A] is a category 2 product. Future Tensor PC models will expand to other categories.

[I20A] SBC

[I20A] SBC is designed to incorporate only the essential functional elements and bring out all available interfaces with maximum flexibility.

[I20A] SBC is based on a platform with a dedicated chipset (CM246, of the same family found in Airtop3) to ensure much more interfaces than available on a SoC-based platform like IPC3 or Whiskey-Lake.

[I20A] SBC supports up to 64 GB DDR4 using 2x SODIMM (dual channel) – with optional ECC for CPUs supporting that.

Performance

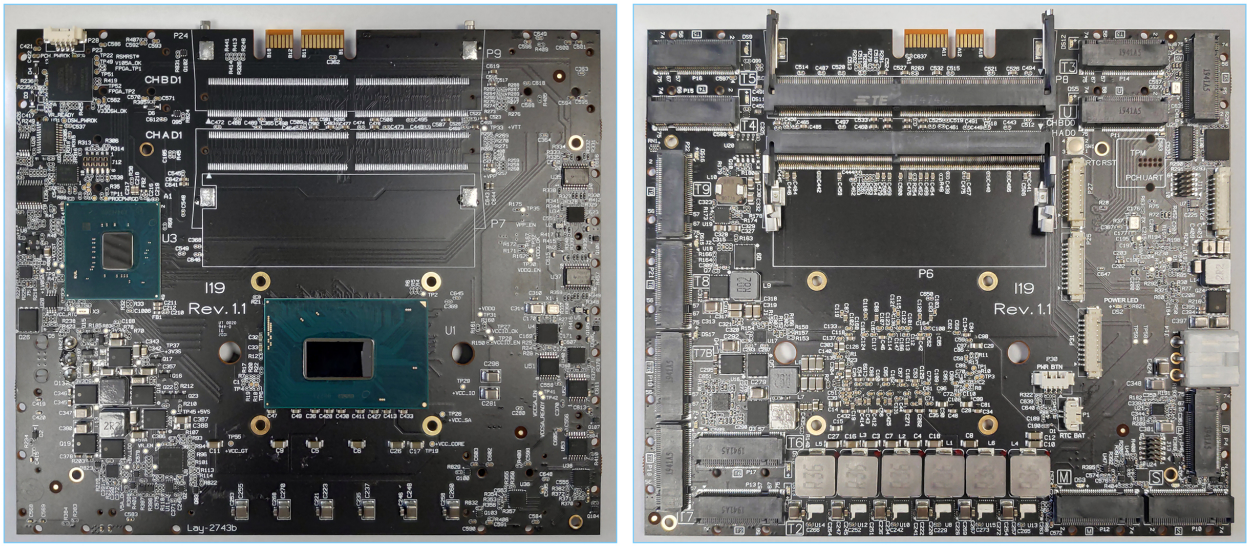
[I20A] is based on Intel 9th generation Core / Xeon "Coffee Lake Refresh" with up to 6 cores.

Performance of the high-end models of [I20A] are about 3 times higher than the performance of Compulab IPC3.

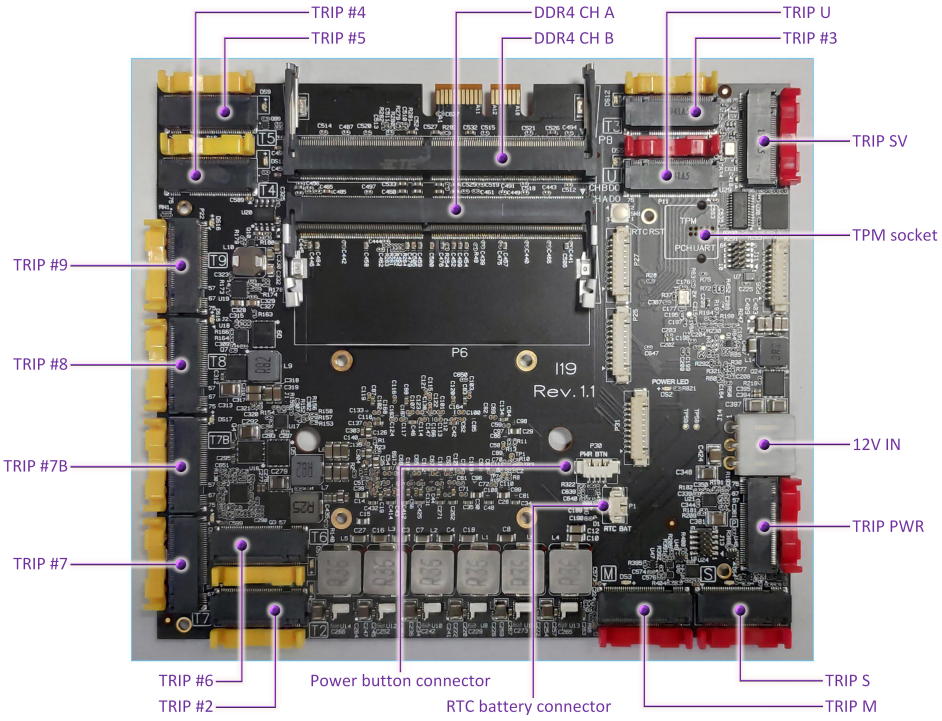
- Performance of the low-end [I20A] is comparable to high-end IPC3.
  This may prove useful for price optimization where no extra performance is required.

[I20A] SBC key features

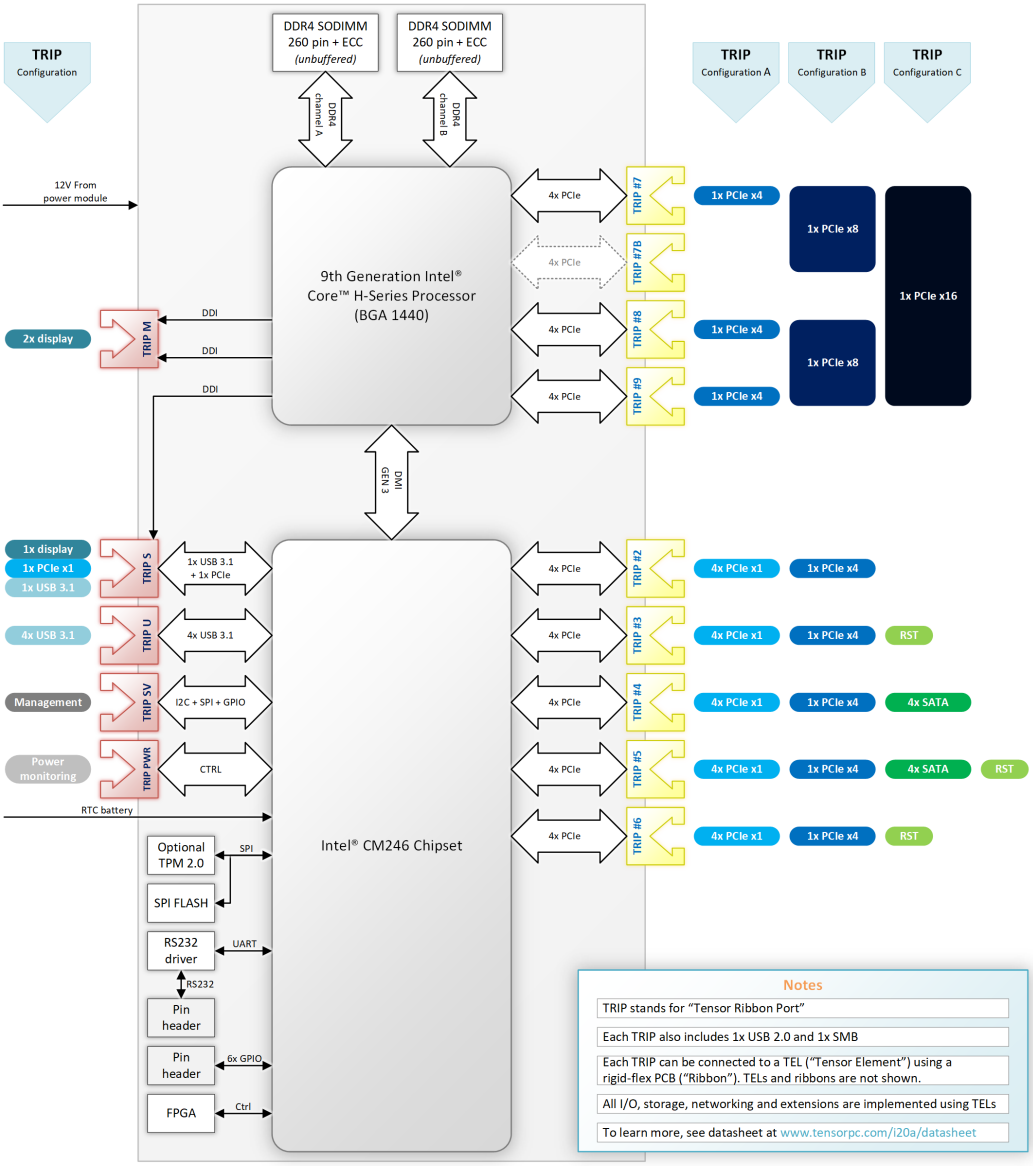
- Intel 9th generation "Coffee Lake Refresh" Core / Xeon up to 6 cores, 25W
- Intel CM246 chipset
- 2x DDR4 SODIMM sockets in dual channel supporting up to 64 GB ECC / non-ECC RAM
- 37 PCIe 3.0 lanes
- 3 display interfaces
- FPGA for power sequencing and control
- Single 12V power input
- TPM 2.0 socket
- Size 15cm x 13cm



[I20A] SBC top and bottom



[I20A] SBC bottom annotated



[I20A] SBC block diagram

Modularity

In Compulab's experience, industrial-PC hardware requirements from the IIOT market are too diverse to meet effectively with a single SBC design.

Back in 2011 Compulab introduced the FACE Module concept with the 1st IPC in order to address this problem. However, the FACE Module allows adding only one type of pre-defined extension card.

Many IIOT projects require multiple types of specific devices and ports. For example – multiple PoE ports, RS485 ports and multiple storage devices required in the same industrial PC. In fact, requirements for multiple custom features has been rising steadily in recent years. Tensor-PC takes a major step forward in addressing this type of diversity, as detailed below.

TRIP (Tensor Ribbon Port)

Just like a FACE Module, TRIP brings out 4x PCIe, but TRIP achieves that using an M.2 connector, which is much smaller. This allows placing multiple TRIPs on the compact [I20A] SBC.

The illustration below shows IPC3 block diagram on the left and [I20A] block diagram on the right, with the modular 4x PCIe interfaces of each highlighted.

There is a single 4x PCIe FACE Module interface in IPC3, where [I20A] has 8 TRIPs, each with 4 PCIe lanes.

To manage the extra complexity of multiple TRIPs, Tensor-PC includes several extra features:

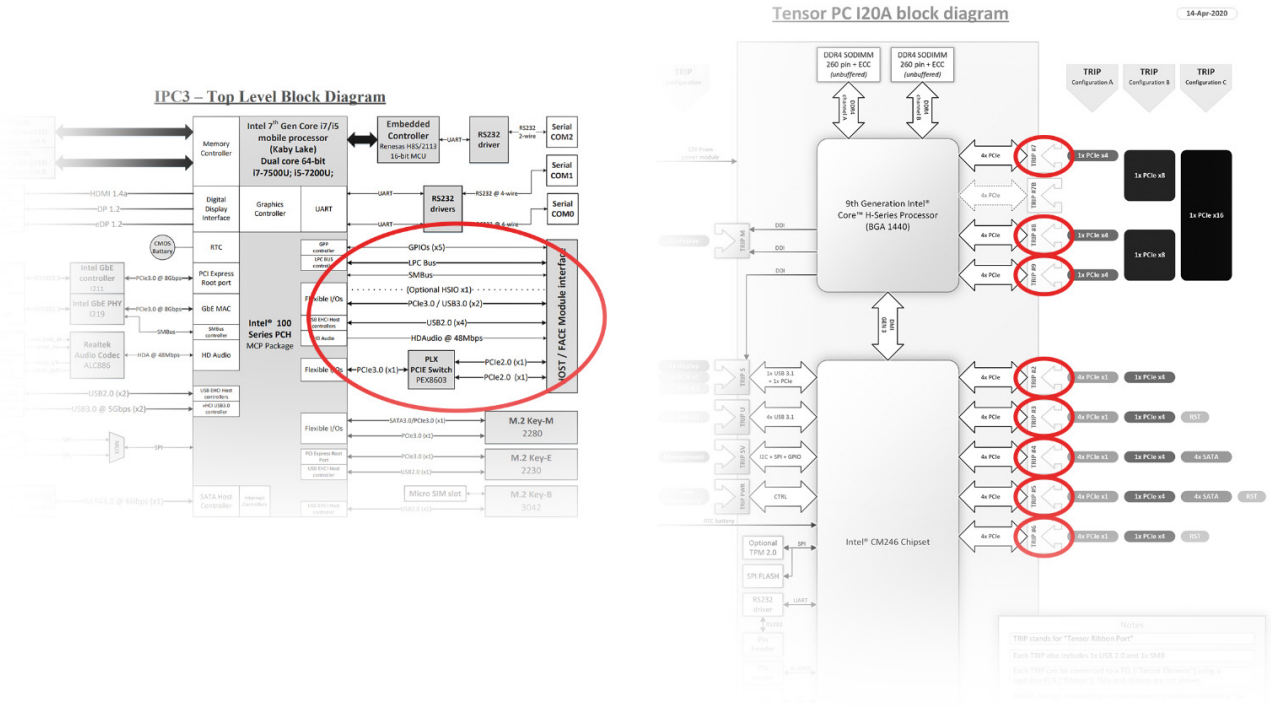
- Identification of the type of TEL connected to each TRIP and the type of Ribbon used
- Provision for enabling or disabling each TEL
- Each TRIP is accompanied by a LED which lights green only if:
  - Connected TEL is detected
  - TEL compatibility to the specific TRIP is verified
  - TEL is enabled

TEL (Tensor Element)

- Each TRIP accepts a TEL which is equivalent in functionality to a FACE-Module
  TEL can have up to twice the functionality of a fitlet2 FACET Card
- Each TRIP can connect to a different type of TEL
- Connecting multiple TRIPs each to a TEL of the same type is also supported

TEL advantages over the FACE Module

- TEL form-factor is usually much smaller than the form-factor of the FACE Module, but if required, TEL can be made larger (e.g. for supporting a hard disk)
- TEL can be installed in any position in any of the four sides of Tensor-PC
- TEL can be ordered separately from Tensor-PC to be assembled by the user
- TEL is easy to install in the field and is held firmly in place with no screws
- TEL is compatible with multiple Tensor-PC models
- Tensor-PC automatically detects which type of TEL is connected to which TRIP and reconfigures itself to support it.
  In case an incompatible TEL is connected to a TRIP it is automatically disabled.
- In case of a faulty TEL it can be easily replaced without the need for an RMA of the whole computer



Highlighted IPC3 FACE Module on the left and [I20A] PCIe TRIPs on the right

The Ribbon

Direct attachment of TEL to TRIP is undesirable for several reasons:

- It would impose restrictions to the size and shape of the TEL – a noticeable limitation of fitlet2 FACET Card
- It would enforce the relative position of the SBC and the coastline of the enclosure – forcing the enclosure to have a given size which limits cooling flexibility and the ability to incorporate oversized devices
- It would limit the ability to reposition the TELs for accessability (e.g. when one side is used for mounting) and for scaling the height of Tensor-PC coastline

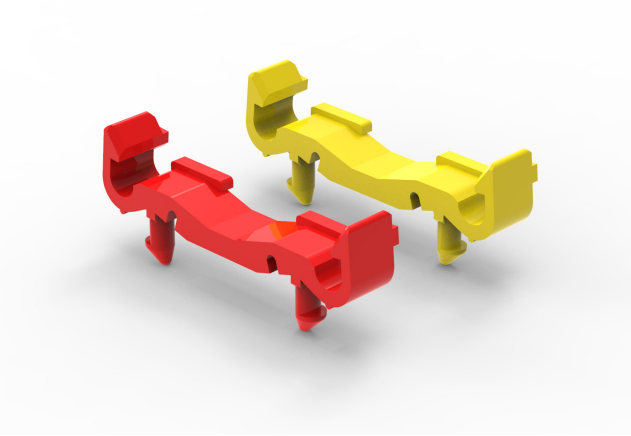
To avoid these limitations found in both FACE Module and FACET Card, Tensor-PC implements a flyover design concept - the TEL connects to the TRIP through a Ribbon.

The Ribbon is a multi-layer rigid-flex PCB which provides complete mechanical decoupling of each TEL from the SBC while maintaining excellent signal integrity, low EMC, small connector footprint, high reliability and easy connection and retention.

Ribbons are available at lengths of 10cm to 30cm to support various enclosure sizes.

RLM (Ribbon Latching Mechanism)

The edge of the Ribbon is pushed into the TRIP M.2 connector. Each TRIP has an adjacent custom-made latch named **RLM** (Ribbon Latching Mechanism). Once the Ribbon is pushed down, the RLM holds it firmly in place.



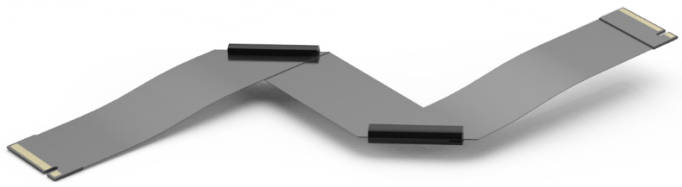
Red and yellow RLMs

RLMs can help distinguishing between TRIPs. PCIe TRIPs have yellow RLMs. Custom TRIPs have red RLMs.

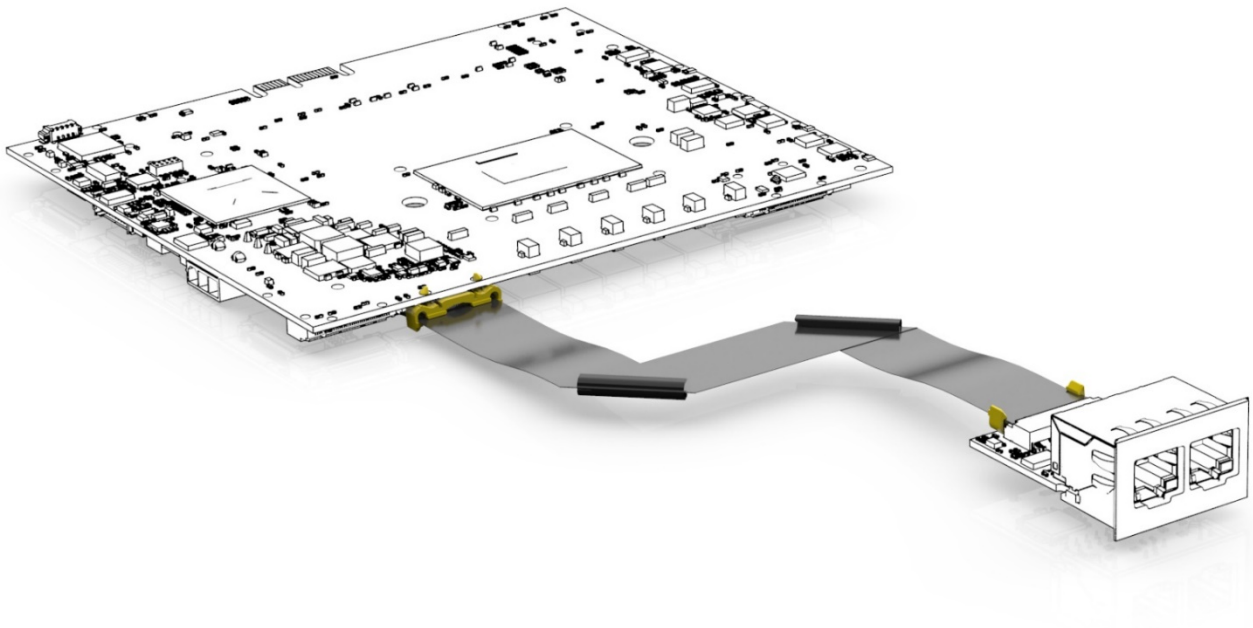
RFC (Ribbon Folding Clip)

Since many ribbons are installed in the confined space of Tensor-PC, keeping the Ribbons organized is important for effective service.

For that, Ribbons can be folded neatly using a custom-made clip named **RFC** (Ribbon Folding Clip).



20cm Ribbon with two RFCs



An illustration of TEL-LANX2 connected by a Ribbon to a TRIP on [I20A] SBC

Types of TELs

It is convenient to categorize TELs to families of storage, power, I/O, networking and extension (SPINE).

Storage TELs

TEL-NVME

M.2 2280 NVMe card or M.2 SATA

TEL-SATAX1

1x 2.5" SSD / HDD

TEL-SATAX4

4x 2.5" SSD / HDD

Additional Storage TELs are in planning phase.

Power modules

IIOT space has a great variety of power input requirements which is next to impossible to meet effectively once the power circuit and power connector are integrated onto the motherboard as is the case with IPC. Tensor-PC is designed with modular power that is added during mechanical assembly.

PM-12V

A miniature 12V power module with polarity, over-voltage protection and twist-lock jack

PM-WIDE

A regulating wide-input voltage, high current power module

PM-BALANCER

A power load-balancer between two inputs for power redundancy

Additional power modules are in planning phase.

I/O TELs

TEL-STD

Display Port + Gbit Ethernet on a single compact TEL, designed for TRIP-S

TELMINIDPX2

2x Mini Display Port, designed for TRIP-M

TEL-DPHDMI

Display Port + HDMI, designed for TRIP-M

TEL-USB3X4V

4x USB3 type A vertical connectors, designed for TRIP-U

TEL-USB3X4H

4x USB3 type A horizontal connectors, designed for TRIP-U in A stacking

TEL-USB2X4V

4x USB2 type A vertical connectors

TEL- USB3X4VPCIE

4x USB3 type A vertical connectors using PCIe to USB3 bridge

TEL-TBX2

2x Thunderbolt 3 with USB type C connectors

TEL-AUDIO

Headphones / line-out + microphone using 2x 3.5mm jacks.
Requires only USB2 interface, does not occupy a TRIP

TEL-SERX4

4x RS232 / RS485 with DB9 connectors.
Requires only USB2 interface, does not occupy a TRIP

TEL-CANBUS

CANbus interface using DB9 connector.
Requires only USB2 interface, does not occupy a TRIP

TEL-GPIO

Up to 20 isolated general purpose I/Os using terminal blocks.
Requires only USB2 interface, does not occupy a TRIP

Additional I/O TELs are in planning phase.

Networking TELs

TEL-LANX2

2x Gbit Ethernet ports using RJ45 connectors

TEL-LANX4

4x Gbit Ethernet ports using RJ45 connectors

TEL-POEX2

2x Gbit Ethernet with PSE PoE using RJ45 connectors.
Requires enclosure with C stacking

TEL-OPLNX2

2x fiber optics Gbit Ethernet using SFP+ sockets.
Requires enclosure with C stacking

TEL-10GBEX2

2x 10 Gbit Ethernet ports

Additional networking TELs are in planning phase.

Extensions TELs

TEL-MINIPCIE

mini-PCIe socket with a panel mounted tray for SIM-card

TEL-M2E

M.2 key-E socket

TEL-M2B

M.2 key-B socket with a panel mounted tray for SIM-card

TEL-PCIE16

Supports full-size PCIe card, PCIe x1 | x2 | x4 | x8 | x16.

- For PCIe x8 TEL should be connected either to TRIP #7 + TRIP #7B or to TRIP #8 + TRIP #9
- For PCIe x16 TEL should be connected to TRIP #7 + TRIP #7B + TRIP #8 + TRIP #9

TEL-SPLITPCIE

Reroutes the four PCIe x1 ports on a TRIP to 4 TRIPs, each with only the first PCIe x1 available.
For example, can be used for connecting four TEL-MINIPCIE to the same TRIP

TEL-SV

a microcontroller-based TEL for out-of-band management and monitoring, designed for TRIP-SV

Additional extension TELs are in planning phase.

Progressive development

Compulab develops TELs progressively according to a dynamic workplan. Not all TELs are available at introduction. Additional TELs that are not listed above would be developed.

Worth noting that developed TELs are compatible with future Tensor-PC models. Models beyond [I20A] would be launched with a large and growing library of TELs.

TELs are open-source hardware

All schematics, bill-of-material, production files and mechanical design of TELs are open and published.

Tensor-PC users are welcome to inspect the TEL design in order to use it better or for identifying design issues.

3rd parties are welcome to design custom TELs and are not required to open-source them. The open-source TELs by Compulab can serve as a reference.

What if there is no TEL with the function I need?

For small projects, the best practice would be to use an extension TEL to incorporate an off-the-shelf card.

It may be worth bringing the requirement to the attention of Compulab technical support. In some cases, there may be a solution present or in the works. In other cases, the feedback about market need may result in Compulab designing a solution.

It is also possible to develop the TEL using hardware design service of a 3rd party. Compulab would provide technical support as required.

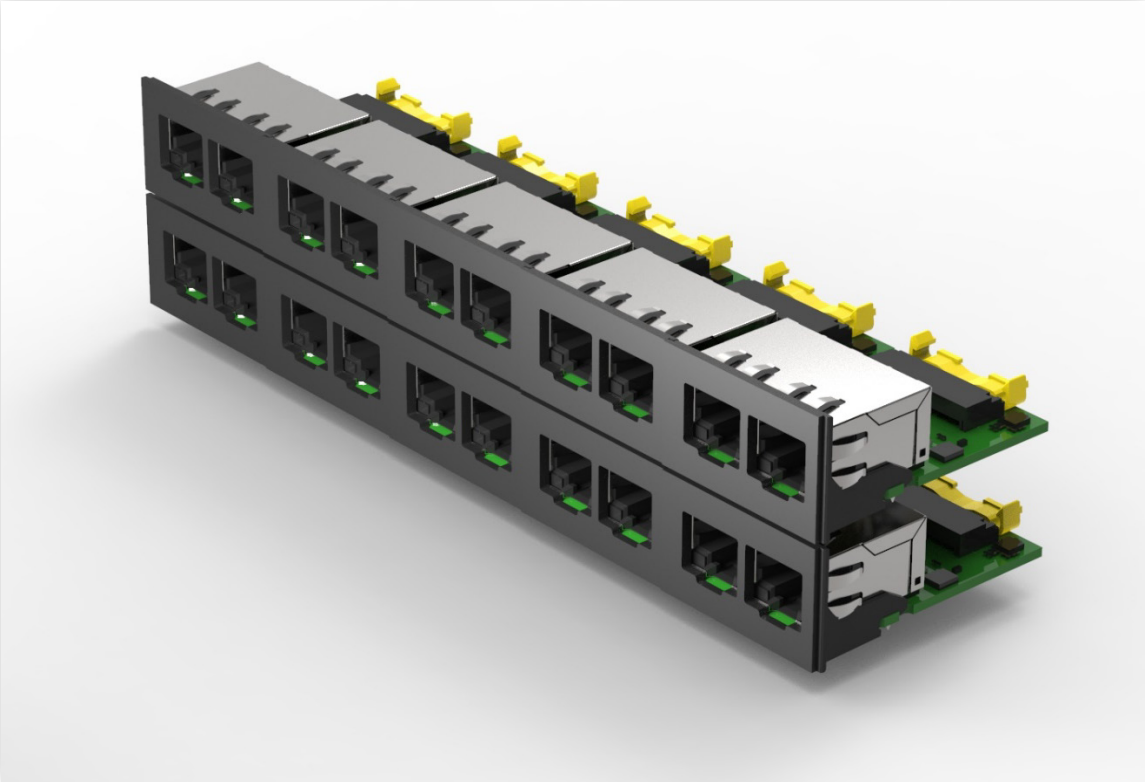
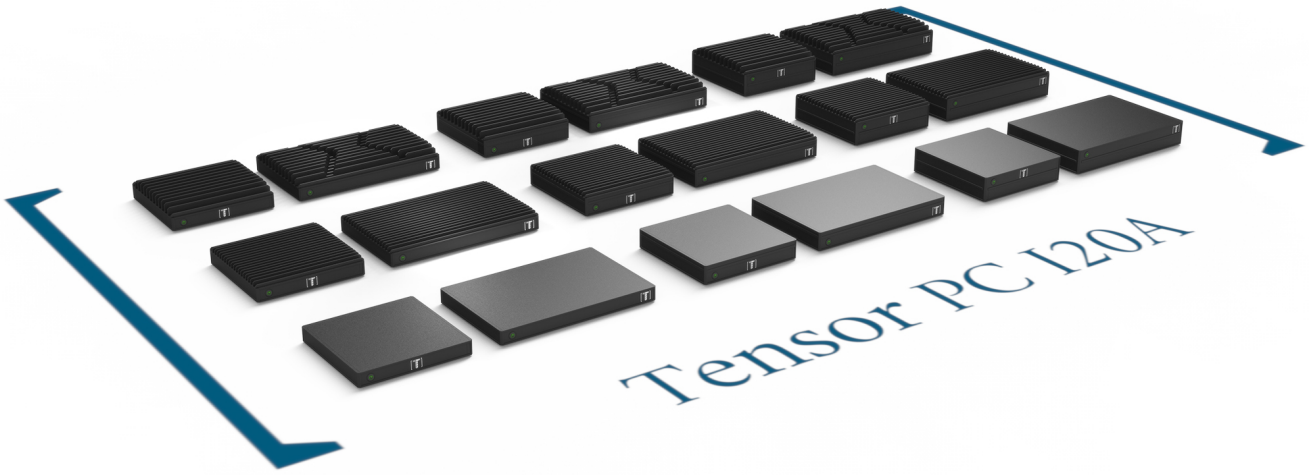


Illustration of 10x TEL-LANX2 in AC stacking

[I20A] enclosure



[I20A] comes in 18 enclosure variants. At first sight this may look overwhelming, but in fact there are just 3 parameters to the enclosure, each can be adjusted independently of the others.

Since all enclosure variants use the same SBC and BIOS, changing to a different kind of enclosure at any stage of the project is straightforward, as well as having more than one kind of enclosure in the same project.

The parameters of the enclosure are:

Width (W)

Width affects space for devices, coastline for ports and cooling capacity.

[I20A] is offered in the following widths:

- 20cm (W20)
- 30cm (W30).

Cooling ribs (C)

[I20A] adopts the top cover options for various thermal scenarios introduced for fitlet2 and extends it.

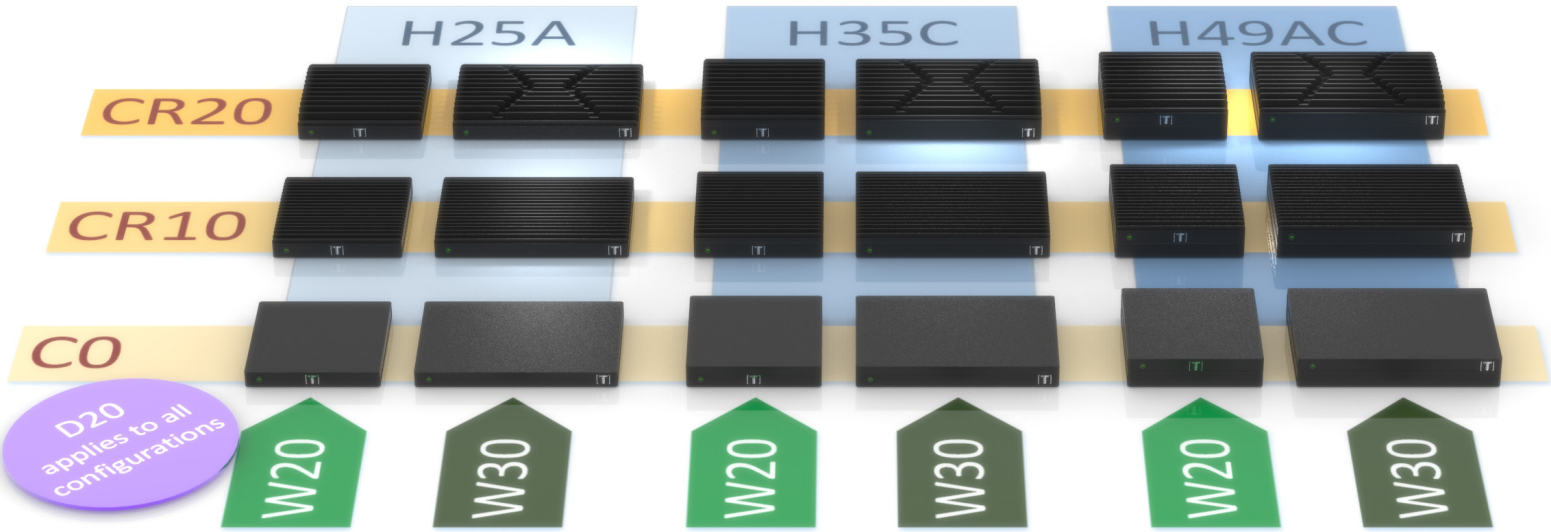
- C0 is a flat top cover for conduction cooling that does not add to the height.
- CR10 provides 10 mm ribs – like the ribs found in IPC and fitlet2, adequate for most indoor / commercial temperature applications.

CR20 provide 20 mm ribs. Extended / industrial temperature [I20A] is offered with CR20.

Compartment height / stacking (H)

Stacking affects space for devices, coastline for ports and the type of devices that can be incorporated.

- Stacking H25A is the thinnest with compartment height of 25mm (excl. cooling ribs), but some devices like optical LAN, PoE and thick hard disks do not fit in this stacking. In A stacking, The SBC is sharing space with TELs. Given skyline of the SBC must be considered when positioning TELs.
- Stacking H35C has a compartment height of 35mm (excl. cooling ribs) and has the SBC out of the way. All [I20A] TELs fit at any position. This is the recommended stacking for ordering [I20A] barebone and DIY.
- Stacking H49AC is a dual layer compartment – an A layer (shared with SBC) and a C layer. H49AC should be considered if more TELs are needed than H35C can accommodate.



Parameters of [I20A] enclosure – width (W), cooling (C) and height (H)

[I20A] 360° coastline and TPU

The total faces of a computer having ports are referred to as "Coastline".

IPC3 coastline is somewhat limited – it has a fixed back panel with a given set of ports, and a relatively small front panel for the FACE Module. There are no ports on the sides.

In [I20A] TELs with ports can be installed 360° - in all 4 sides of the coastline on the full length of each side.

TPU (Tensor Panel Unit)

To assist in planning of TEL placement, Tensor-PC defines a coastline length unit named **TPU** (Tensor Panel Unit).

1 TPU = 11.15 mm

- Each TEL has a width of an integer number of TPU.
  For example: TEL-LANX2 with 2x RJ45 has a width of 3 TPU (33.45 mm)
- Each side of [I20A] has a length of an integer number of TPU
  For example: [I20A]-W20-D20-H25A-CR10 has 16 TPU on each of its 4 sides for a total coastline of 64 TPU
- By the example above, each side of [I20A]-W20-D20-H25A-CR10 could fit **(int) 16/3 = 5** TEL-LANX2 on each side.
  If we were to populate all 4 sides with TEL-LANX2, then 5x4 = 20 TEL-LANX2 which would allow 40 RJ45 ports.

Note: The example above is for coastline illustration only. Availability of TRIPs must also be considered.

If coastline is insufficient

It is a good practice to configure with spare coastline for several reasons:

- During project development it is often found that extra features are needed.
  For example, changing storage device from M.2 (2 TPU) to a 2.5" SSD (7 TPU)
- There are some practical limitations in TEL placement. For example, Two TELs in a corner would interfere with each other
- Effective port organization has cables on the back, buttons and plug-in ports on the front, antennas on the back or on the side. Coastline that is too short may result in awkward compromises that may lead to poor customer satisfaction and difficult integration
- Many TELs in a small space makes assembly and service difficult
- Once [I20A] is side-mounted, coastline is reduced

Coastline can be increased by 25% by changing width from W20 (64 TPU) to W30 (80 TPU).

Coastline can be increased by 100% by changing stacking from H25A (64 TPU) to H49AC (128 TPU).

[I20A] cooling performance

Effective fanless cooling is the major differentiating factor between a commercial PC and an IIOT platform.

[I20A] has a more advanced fanless cooling than the older IPC family.

- CPU cooling is based on heatpipes rather than on a solid copper block like in IPC
- Buyer can adjust the trade-off between a smaller footprint and higher cooling capacity (by enclosure parameters C and W)
- In [I20A] the CPU frequency and power are preset to match the cooling capacity of the selected enclosure.
  Note: user can change CPU frequency preset
- Some TELs include thermal coupling for effective cooling of specific devices (e.g. storage devices)

Industrial temperature range

Tensor-PC introduces several new features specifically designed for supporting extended (TE) and industrial (TI) ambient temperature range:

- [I20A] TE/TI are built differently from commercial temperature [I20A]:
  - Enclosure with more thermal headroom
  - Use of premium thermal interface materials (TIMs)
  - Industrial grade storage devices only
  - **Note**: Each TE/TI [I20A] undergoes testing at extreme temperatures
- [I20A] TE/TI has an optional pre-heating feature to ensure successful power-up in cold ambient temperature

TIPP (Industrial Temperature Predictable Performance)

An IIOT PC must not enter thermal shut down within designated temperature range. This is provided by TI rating.

It is also desirable that performance is not reduced at high ambient temperature. This was never an option with older Compulab computers but is now an option with [I20A]. This option is called TIPP rating.

Detailed discussion about TIPP is beyond the scope of this document.

Integration and mounting

Mechanical mounting is a key requirement in many IIOT integration projects. IPC3 has the VESA mounting bracket with DIN-rail adapter that allows mounting it from the bottom side for convection cooling.

[I20A] can be mounted as follows:

- Bottom mounting to VESA, DIN-rail or wall
- Side mounting to DIN-rail or wall
- Top mounting with C0 top cover (like fitlet2 industrial top cover) for conduction cooling

Details of mounting fixtures are beyond the scope of this article.

Implications of Tensor-PC design on reliability

Reducing RMA

IPC is designed for serviceability and allows replacing storage RAM and add-on cards in the field. However, most of the features are integrated on-board, so in case of a failure of a port – the whole computer must be sent back by RMA for repair.

In [I20A] the SBC features are reduced to the bare minimum, where all SPINE is implemented on TELs which can be easily replaced in the field.

Reducing downtime

Since TELs are relatively inexpensive, it is possible for a customer to order a replacement TEL and get refunded for the faulty one, rather than waiting for the round-trip time of a full RMA. It may be commercially viable for integrators and resellers to keep inventories of spare TELs for quicker replacement in the field.

In mission-critical [I20A] projects, SNIPE TELs can be pre-installed in redundancy and be toggled on/off in case of a fault.

Reducing penalty of errata

Sometimes an erratum is discovered after many units are deployed in the field. This is one of the most difficult and expensive technical issue to address.

In [I20A] the likelihood of an erratum related to the SBC is significantly lower than in IPC, because much of the design complexity is moved from the SBC to the TELs.

An erratum in a TEL does not require an RMA and is much cheaper and quicker to fix.

Customization services

Compulab has hardware and software development, product design and production taking place under the same roof.

This allows Compulab to offer a wide range of customization services.

Most of the customization services are affordable even for relatively small orders.

Compulab fitlet2 makes a good example of the customization services Compulab can offer, including:

- Product re-branding
- BIOS customization
- Custom painting
- Custom labeling
- OS imaging
- Custom reporting
- Custom packaging

With Tensor-PC Compulab is offering all the services above and adds some new ones:

Laser marking on the enclosure

- QR codes
- MAC addresses
- Application specific port labeling etc.
- Logo

Note: Compulab has in-house laser marking capability so this option is available at a low MOQ.

Enclosure customization

- Change in width (W)
- Change in stacking (H)
- Change in cooling ribs (C)

This option becomes possible thanks to the parametric design of [I20A]. In most cases it will not require expensive new tooling.

TEL customization

Since TEL development is much simpler than SBC customization, the minimum-order-quantity of [I20A] that would allow Compulab to design a custom TEL is significantly lower than hardware customization of previous Compulab products.

TELs can also be designed by a 3rd party with Compulab support using existing Compulab TELs as reference.

Glossary

(I20A)

Abbreviation for **Tensor-PC-I20A.**
The first Intel-based Tensor-PC model introduced in 2020.

FACE Module

Acronym for **Function And Connectivity Extension Module**.
The extension card of Compulab IPC family.

fitlet

A family of Compulab miniature industrial PCs (category #1) introduced in 2015.

IPC

Acronym for **Intense PC**.
A family of Compulab industrial PCs (category #2) introduced in 2011.

Ribbon

A rigid-flex PCB that connects **TEL** to **TRIP**.

RFC

Acronym for **Ribbon Folding Clip**.

RLM

Acronym for **Ribbon Latching Mechanism**.

SPINE

Acronym for **Storage, Power, I/O, Networking, Extension cards** which are all the families of TELs that can be installed in Tensor-PC.

TEL

Acronym for **Tensor Element**. An extension card for Tensor-PC.
Multiple TELs can be installed at the same time.

TIPP

Acronym for **Industrial Temperature Predictable Performance**.
A configuration that can operate at a given ambient temperature without throttling the CPU.

TPU

Acronym for **Tensor Panel Unit**.
The width of TELs and the width of each Tensor-PC face are both integer multiple of TPU.

TRIP

Acronym for **Tensor Ribbon Port**. The standard extension port of Tensor-PC.
Each Tensor-PC has multiple TRIPs.