DC-MHS R1 Overview

- Datacenter Modular Hardware System Revision 1.0

Connect. Collaborate. Accelerate.

OPEN Compute Project®

The DC-MHS R1 Mission

- **What:** **D**ata **C**enter – **M**odular **H**ardware **S**ystem Revision 1.0

  DC-MHS R1 envisions interoperability between key elements of datacenter, edge and enterprise infrastructure by providing consistent interfaces and form factors among modular building blocks.

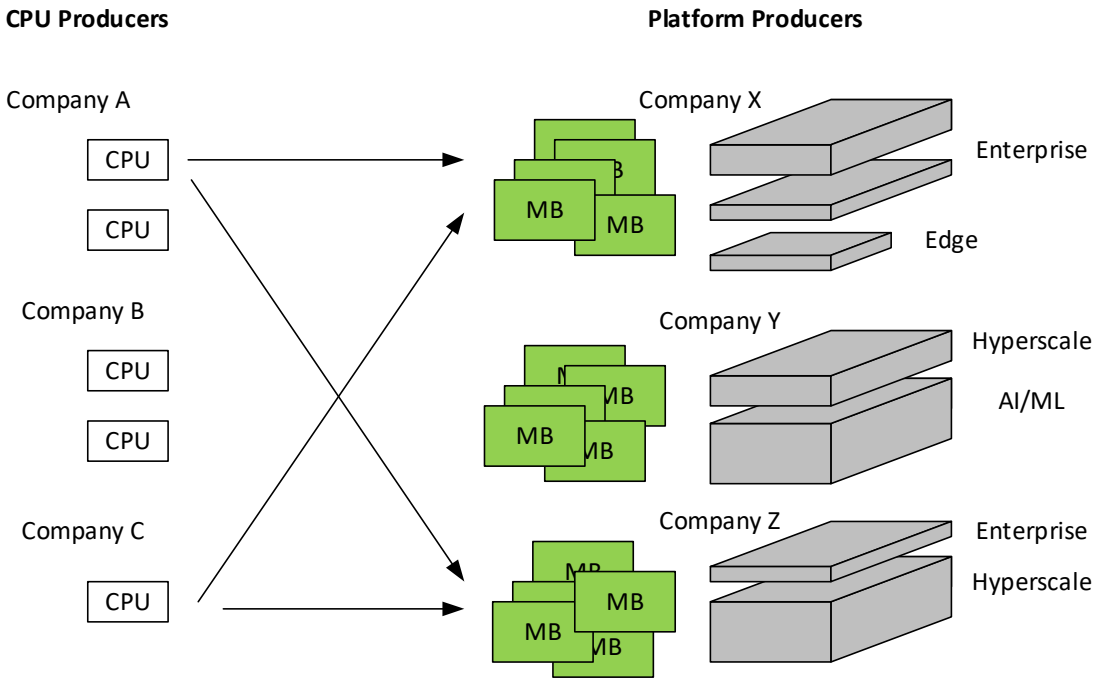
  DC-MHS R1 standardizes a collection of HPM (Host Processor Modules) form-factors and supporting ingredients to allow interoperability of HPMs and platforms.

- **Why**
  1. DC-MHS R1 aims to ultimately improve industry efficiency and innovation.
     - Enable the CPU Suppliers to design and validate the circuit board under their CPUs
     - While preserving the ability for the rest of the supply chain to innovate beyond the CPU
  2. CPU Suppliers are enabled to innovate without barriers to adoption.
  3. Platform Suppliers may innovate without burden of redesigning HPMs
- **When:** Enabling for producing solutions late 2023, early 2024.
- **Who:**

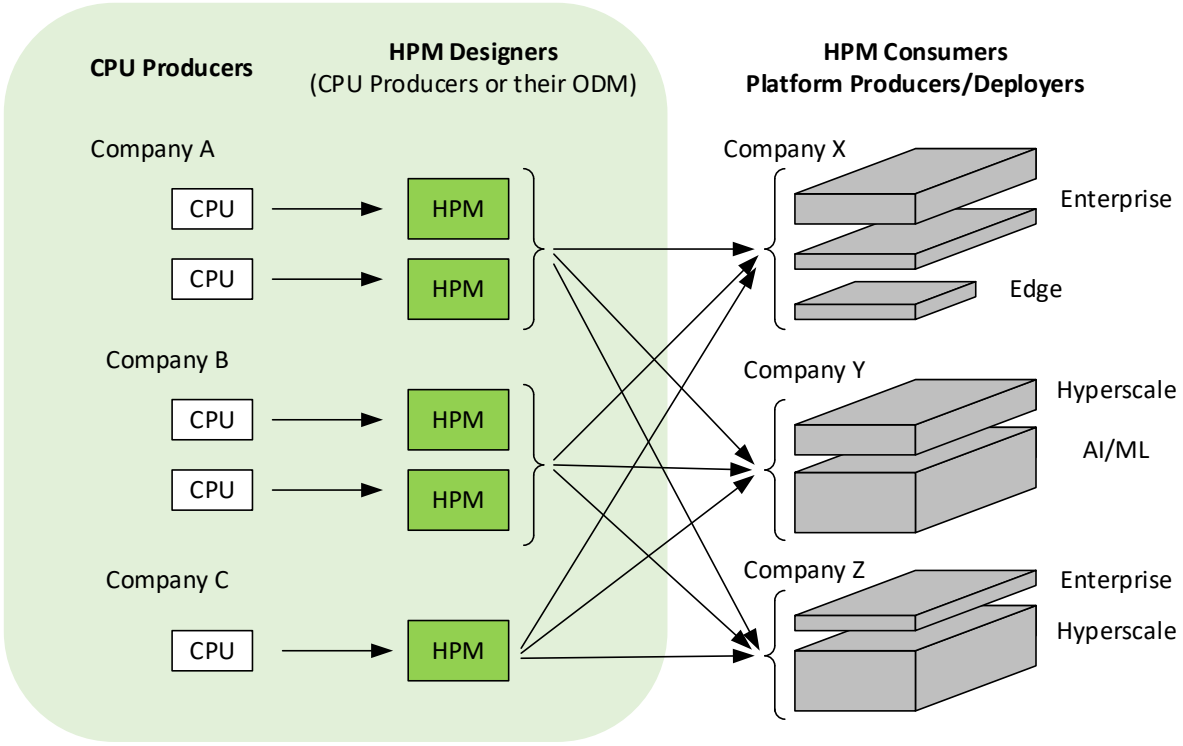
DELL Technologies Google Hewlett Packard Enterprise intel Meta Microsoft

OPEN Compute Project®

Today's Model



New Model w/ DC-MHS



Connect. Collaborate. Accelerate.

HPM Usage Models

HPM As-Is

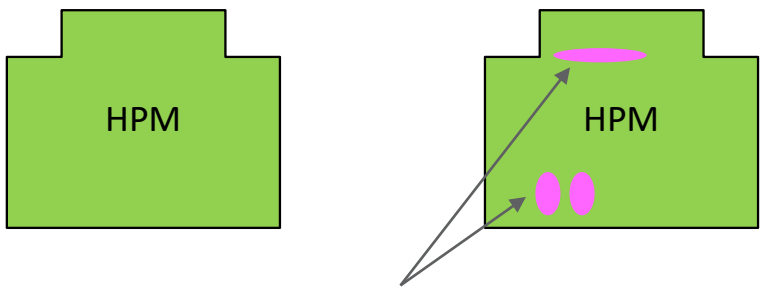
- *All required elements of DC-MHS specs are implemented*
- *Fits into any DC-MHS compliant chassis*

HPM with Value-Add Modifications

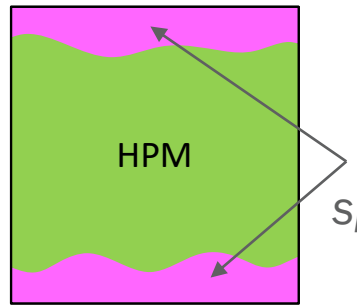
- *All required elements of DC-MHS specs are implemented*
- *Fits into any DC-MHS compliant chassis*
- *Additional capabilities added to HPM for unique offering or applications*

Adapted HPM

- *Based on a DC-MHS compliant HPM "core"*
- *Modifications made that transcend the DC-MHS specs to enable a new application*
- *May not fit into a DC-MHS compliant chassis*



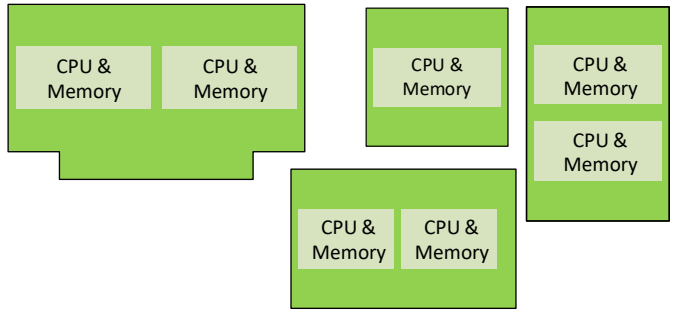
Added capabilities unique for application or Platform Producer

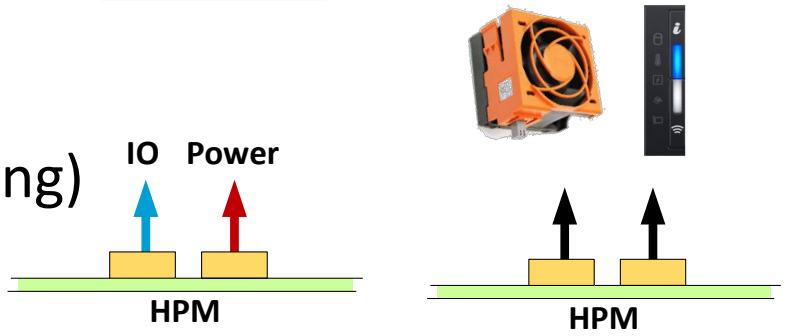


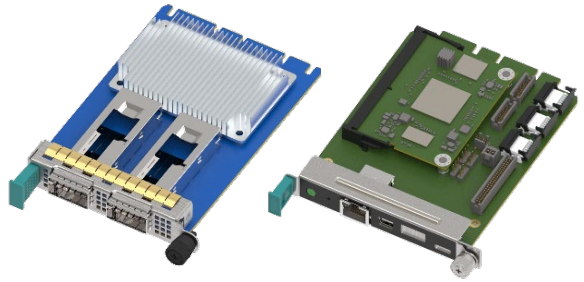
Extensions to HPM adapting it for a specialized application not in specs

Ingredients

- HPM Form-factors:
  - Dimensions, mounting, KOs, Connectors
- Power Supply:
  - Form-factor
  - Electrical operation
- System Connectivity (conn's, pins-outs, signaling)
  - PCIe/CXL, cabled and riser
  - Sideband Virtualization
  - Power Distribution
  - Control Panel
- Utilization of OCP NIC R3 and DC-SCM R2

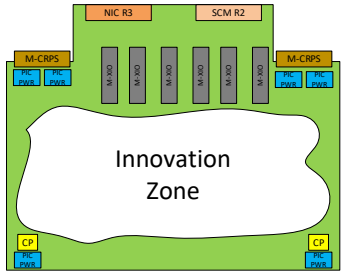




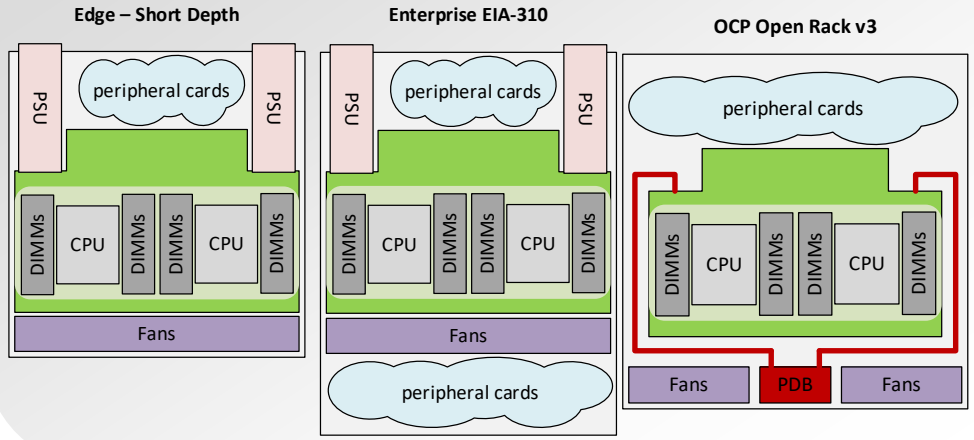


HPMs and Platform Vision

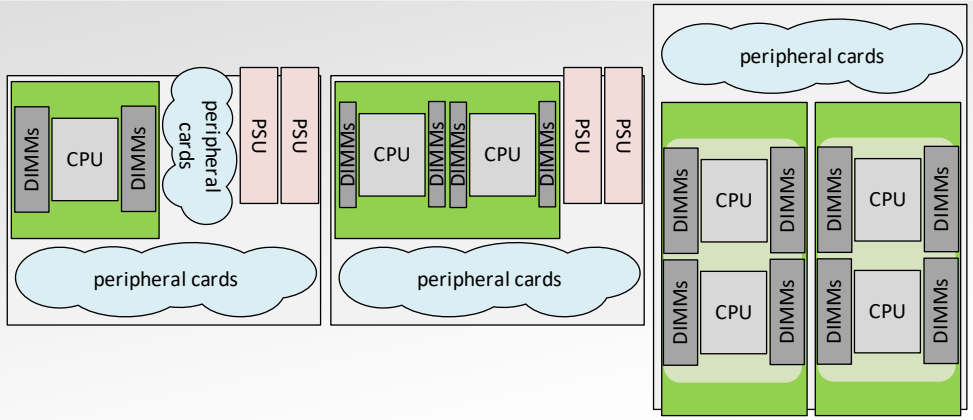
- HPM form-factor specs FLW/DNO match to conventional CPU configs and platform usage.
- However……
- CPU/memory/VR is **NOT** defined by DC-MHS
- HPM Designers may use the form-factor base specifications for other purposes, or larger CPUs.
- HPM form-factors are **NOT** restricted for any rack, targeted at EIA-310 and Open Rack v3



Full Width Form-Factors (M-FLW)
Typically for 2-CPU configurations
Traditional EIA-310 or Open Rack



Density Optimized Form-Factors (M-DNO)
Partial width including "½ Width" 1S, 2S Multi-node, or "¾ Width" 1S/2S
Broad applicability to Rack, Appliances, Multi-Node, and Edge



Documentation, Contacts

- Version 0.7 of DC-MHS R1 is now available at www.opencompute.org/wiki/Server/Working

- Feedback on version 0.7 will be accepted until May 24th, 2022 (prior to May Server Project meeting)
- Send feedback or questions through any of the six DC-MHS company leads listed below, or to the group reflector at dcmhs@opencompute.org
- Version 1.0 of all six of the DC-MHS specifications is targeted for Q3'2022.

Dell	Shawn Dube	shawn.dube@dell.com
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HPE	Jean-Marie Verdun	verdun@hpe.com
Intel	Brian Aspnes	brian.d.aspnes@intel.com
Meta	Todd Westhauser	twesthauser@meta.com
Microsoft	Mark A. Shaw	mashaw@microsoft.com

Q & A

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Next up

@ 8:55 PDT

M-FLW	Full Width Form-Factor HPM
M-DNO	Density Optimized Form-Factors
M-PIC	Platform Infrastructure Connectivity
M-XIO	Extensible I/O
M-PESTI	Peripheral Sideband Tunneling Interface
M-CRPS	Common Redundant Power Supply

DC-SCM 2.0

Q&A and Discussion

Full Width Form Factor (FLW) HPM

as part of DC-MHS Family

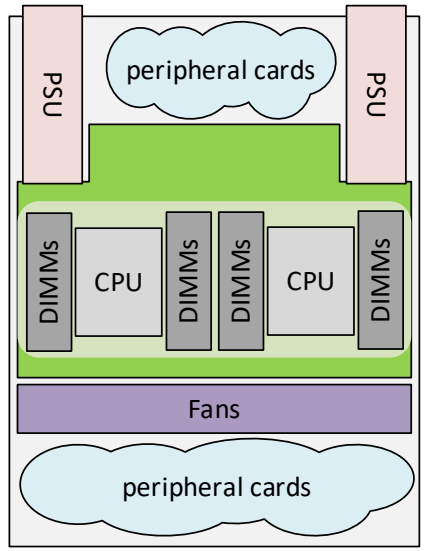
Corey Hartman

Brian Aspnes

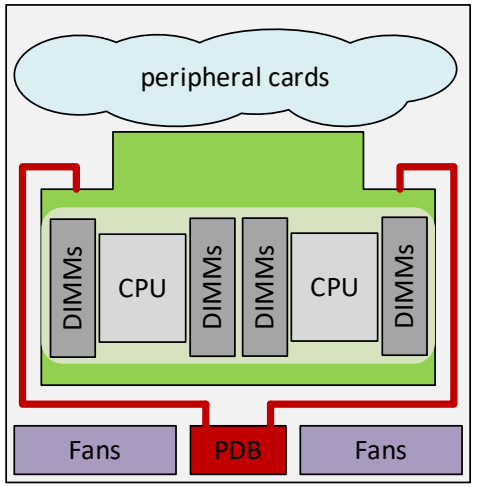
M-FLW HPM “Tenets”

1. Full Width HPM (16.66” Wide) in common racks
   - 19” (EIA-310-D) or 21” (Open Rack v3)rack chassis
2. OCP DC-SCM r2.0 + OCP NIC r3.0
3. Common CPU/Mem Configurations
   - 1-2 socket CPU layouts and maximum IO breakout
   - 1U and 2U chassis configurations
   - DC-SCM r2.0 on hot or cold aisle architectures
4. Compute aspects left flexible (not in scope)
5. Multi-generational chassis re-use
6. Enable air and liquid cooling solutions
7. This is a **Base Spec** and relies on other DC-MHS Base specs for full guidance
   - M-CRPS, M-XIO, M-PIC, M-PESTI

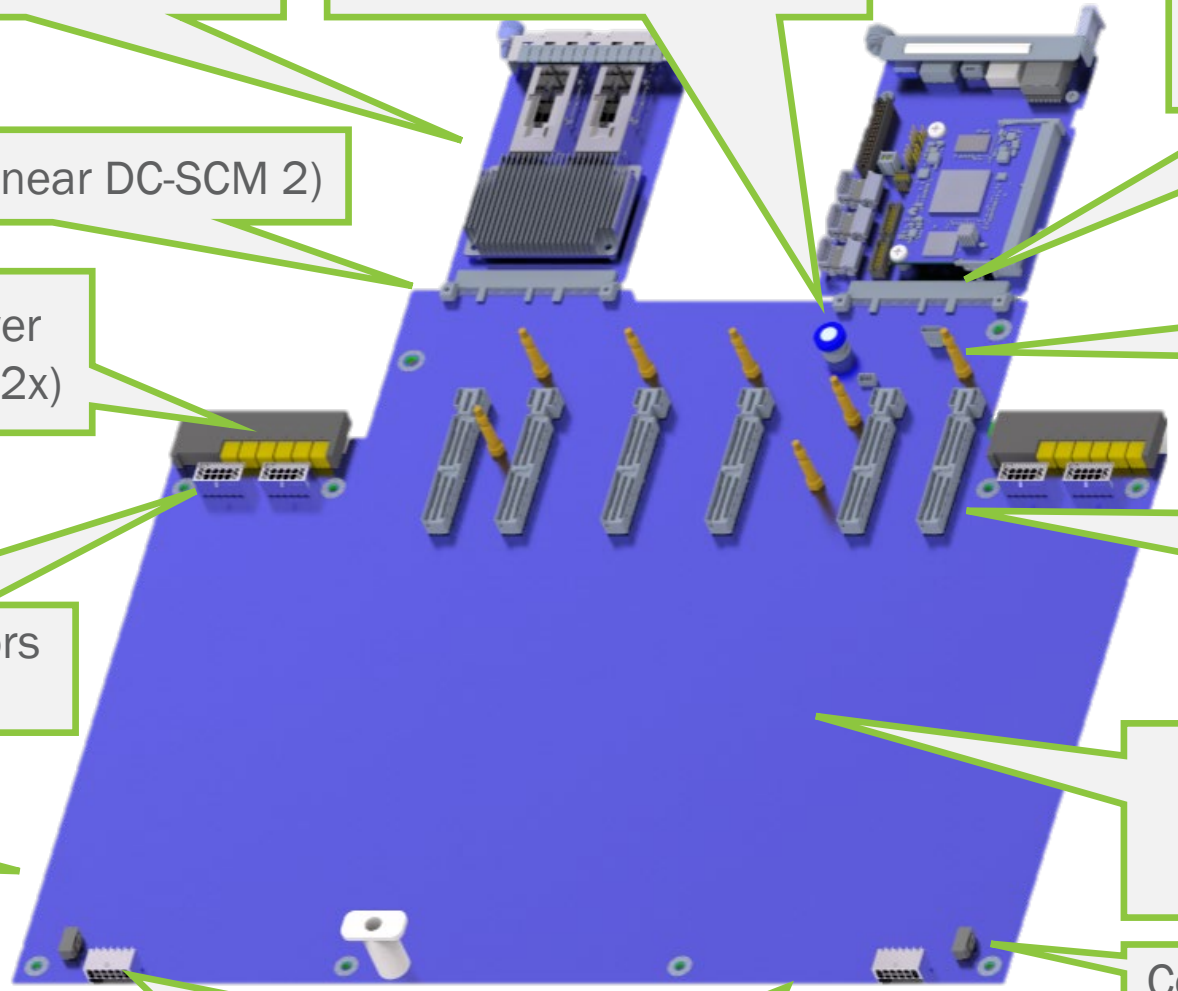
Enterprise EIA-310



OCP Open Rack v3



M-FLW Spec Scope Overview



OCP NIC 3.0 Connector Location

Mounting and Retention Hole Locations

DC-SCM 2.0 Connector Location

Near Side Edge (near DC-SCM 2)

M-CRPS (Ingress) Power Connectors Locations (2x)

Misc Connectors
(Intrusion, USB, Boot)

Fixed Cable or Riser XIO Connector Locations

Egress Power Connectors Locations (4x)

Component height restrictions, keep out zones, etc.

Board Type Outline

Control Panel (2x)

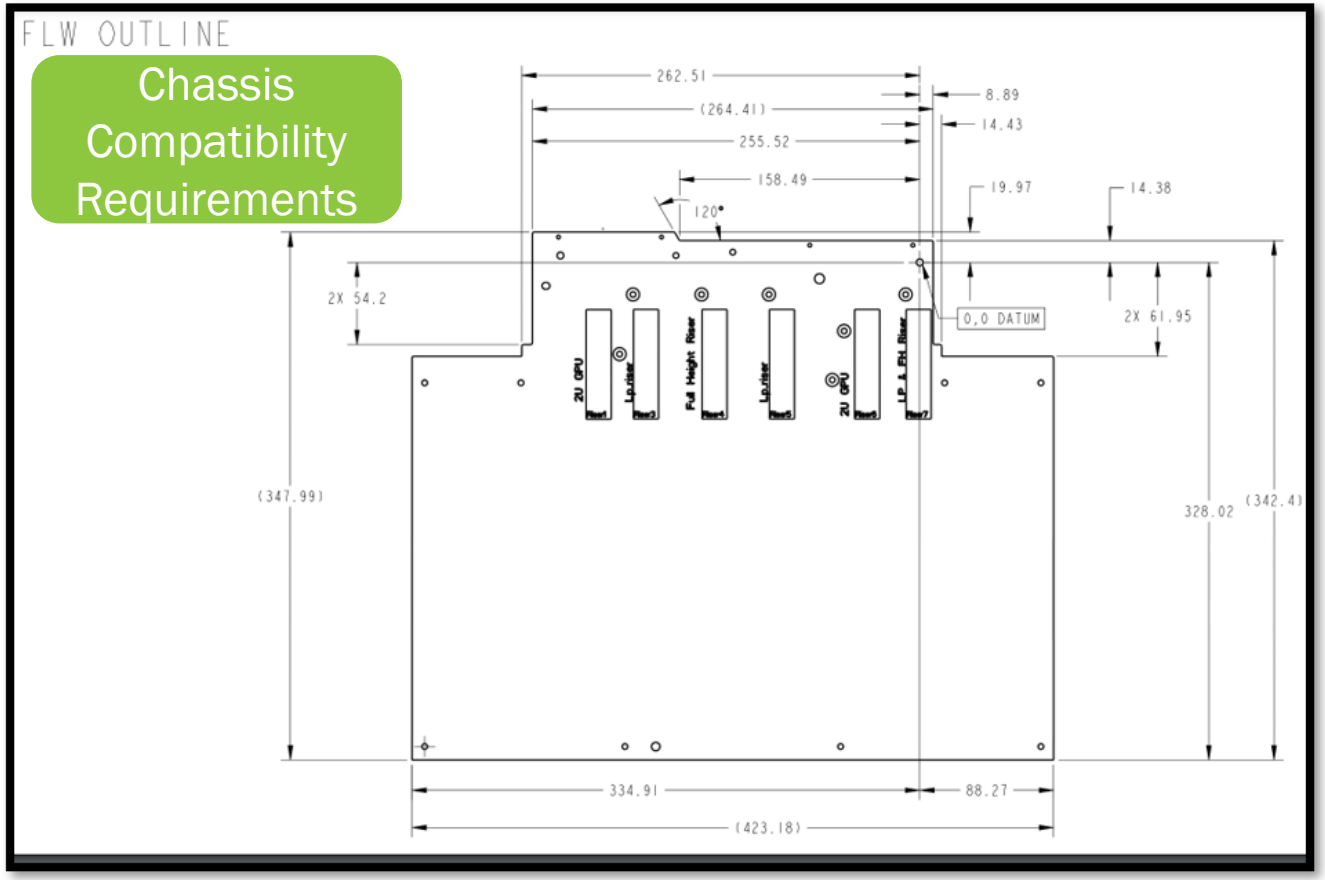
Egress Power Connectors Locations (2x)

Far Side Edge

Connect. Collaborate. Accelerate.

Example Views from M-FLW Spec

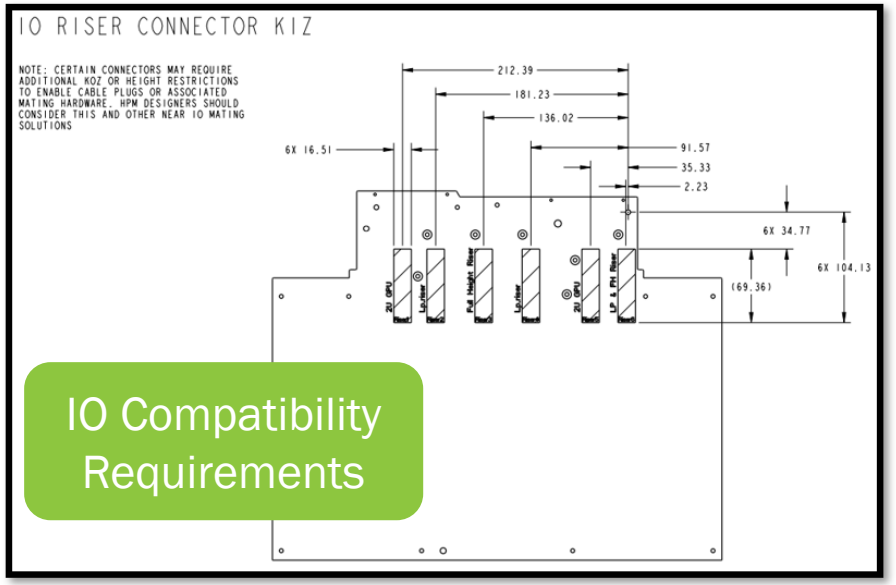
Figure 3. Full Width HPM Outline



Chassis Compatibility Requirements

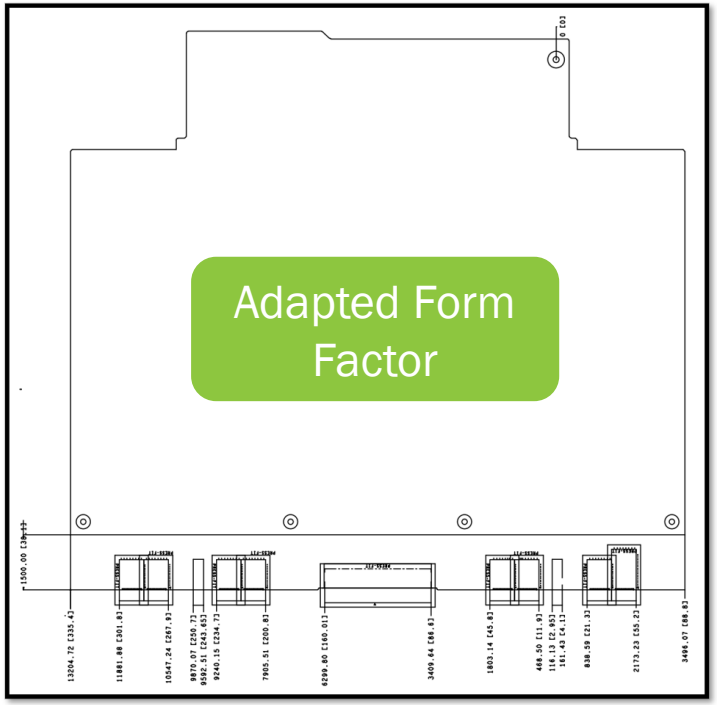
16.66” wide

Figure 15. Near IO Riser-Cable Connector Keep In Zone for Risers



IO Compatibility Requirements

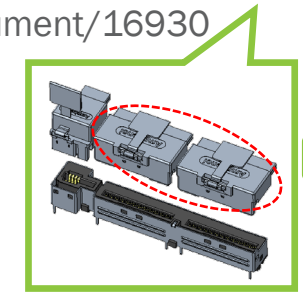
Figure 29. Full Width HPM Outline for UBB Blade FLW



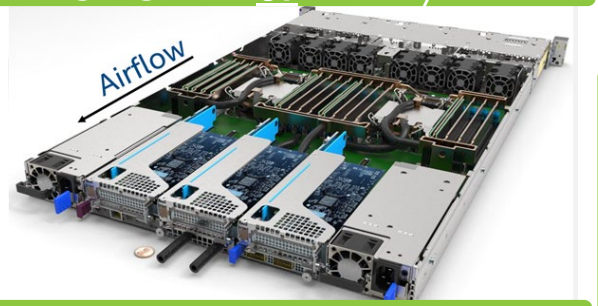
Adapted Form Factor

PCIe/CXL Assumptions

- Enable Common Configurations Shown
  - 180W per x16 Riser XIO (allows for 2x8)
  - Minimize PCIe/Power Required Cabling
- Near Side IO (6x16 XIO Connectors)
  - Support optional cabling 32L to Far Side
  - XIO connectors aligned with PCISIG Cable Spec
    https://members.pcisig.com/wg/PCI-SIG-WG_Members/document/16930
- Far Side IO (undefined)
  - M-FLW does not define Far side XIO
  - Intended to be cabled if placed



1U: 3x LP or 2x FH/HL



2U: 6x FH/FL or 3x DW

Hot Isle Peripherals

1U: 3x LP or 2x FH/HL

2U: 6x FH/FL or 3x DW

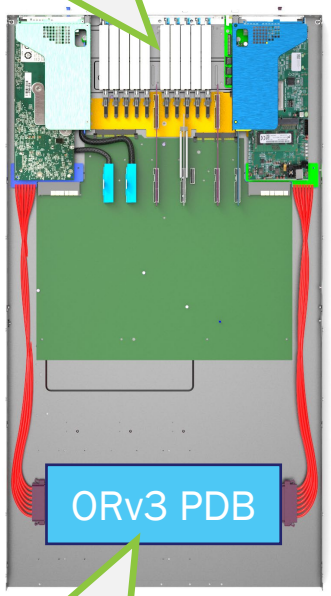
Cold Isle Peripherals

Chassis Front

"U" = 44.45mm

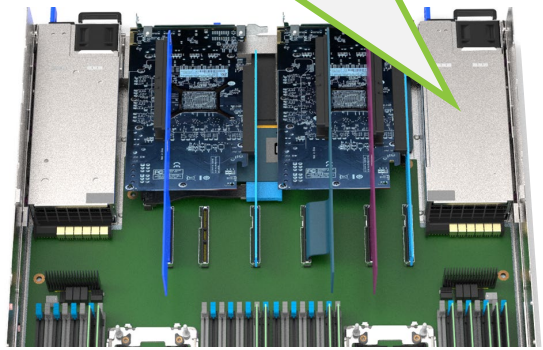
HPM Power

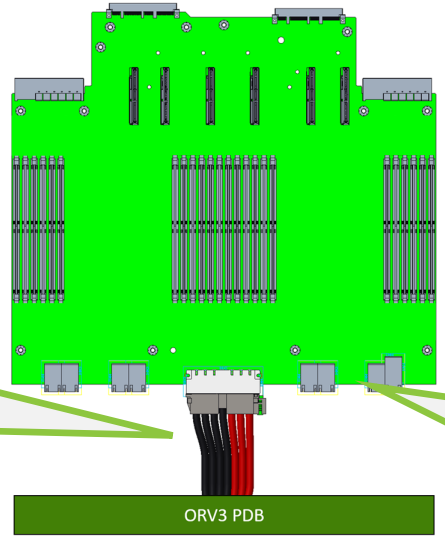
Open Rack v3 Peripherals Reshuffled for 21”



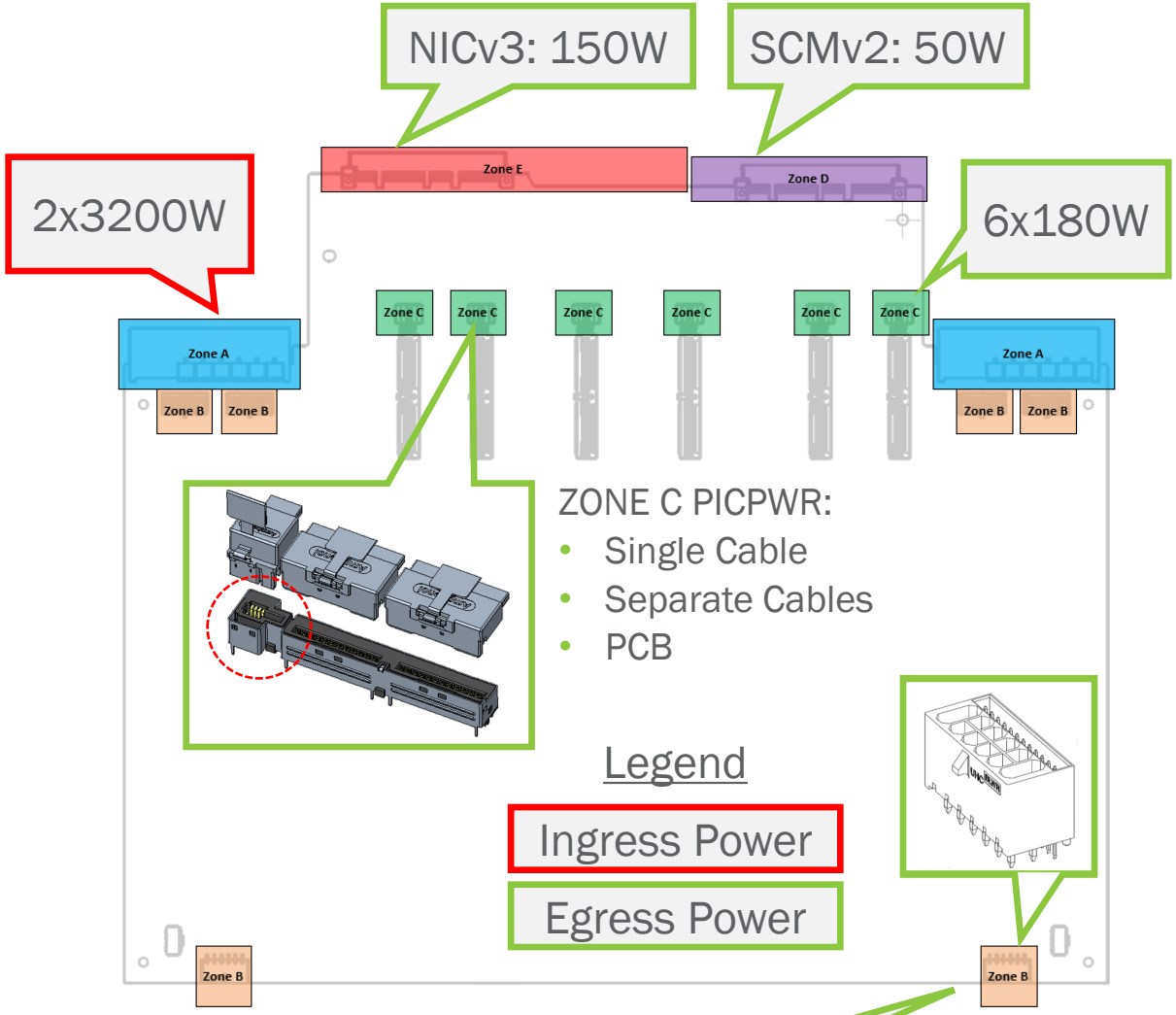
Ingress power can be delivered to HPM from PDB

Ingress Power Direct Dock M-CRPS





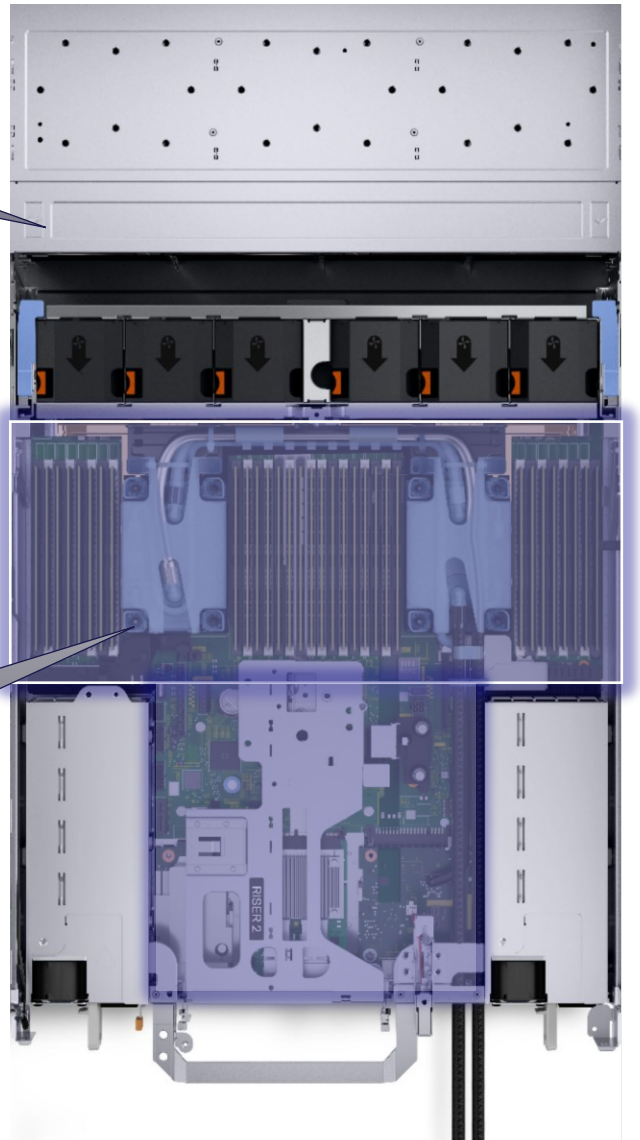
Adapted HPM “Future UBB w/ ExaMAX”



Connect. Collaborate. Accelerate.

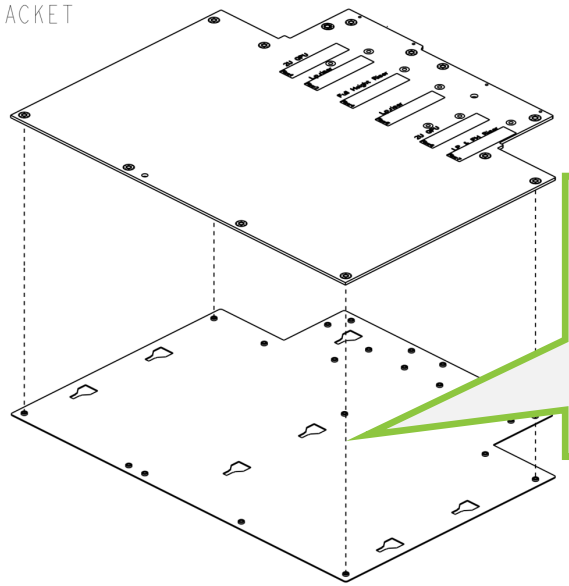
Specifications are Written for Chassis Ecosystem Reuse

Example chassis, not MHS related



Hypothetical HPM

Spec goals: Chassis designed to MHS interfaces may accept new HPM's for 3 Platform Architecture Generations



Chassis-to-board pan

Allows same enclosure, multiple HPMs
(recommended, not required)

Contact Us

- Feedback on version 0.7 will be accepted until May 24th, 2022
- Send feedback or questions to
  - corey.hartman@dell.com
  - brian.d.aspnes@intel.com
  - DC-MHS group reflector at dcmhs@opencompute.org
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Q & A

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DC-SCM 2.0

Q&A and Discussion

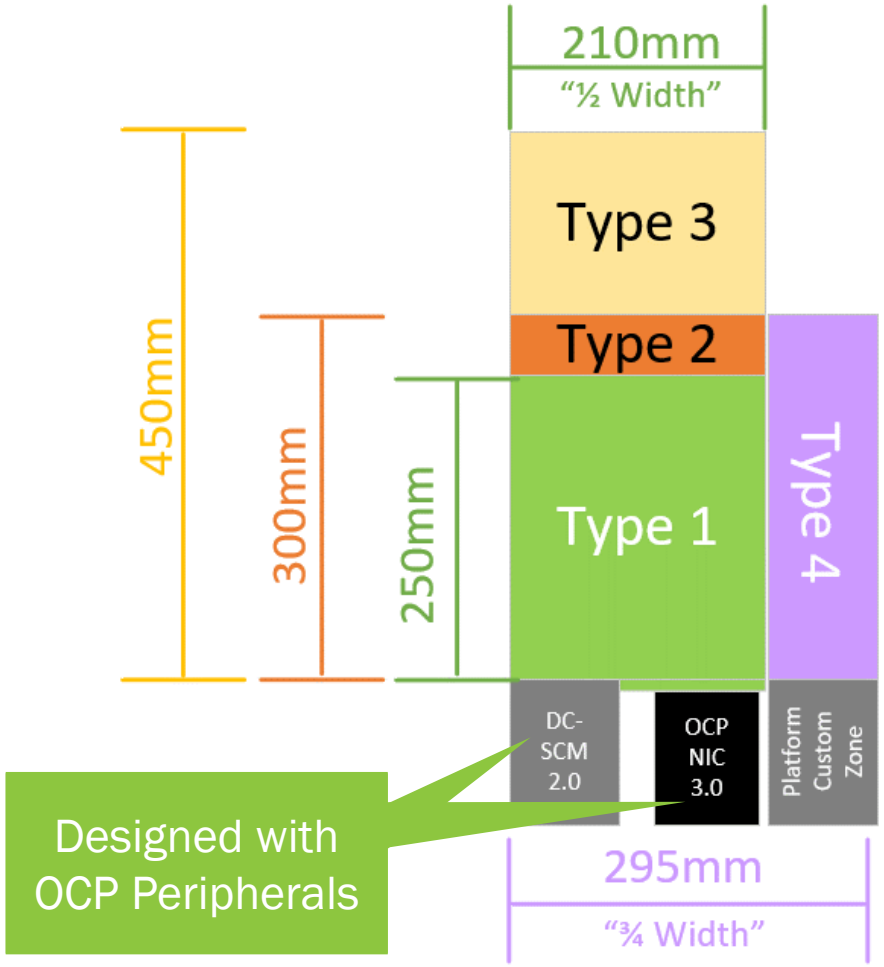
Density Optimized Form Factor (DNO)

as part of DC-MHS Family

Dirk Blevins

Mike Gregoire

M-DNO Overview

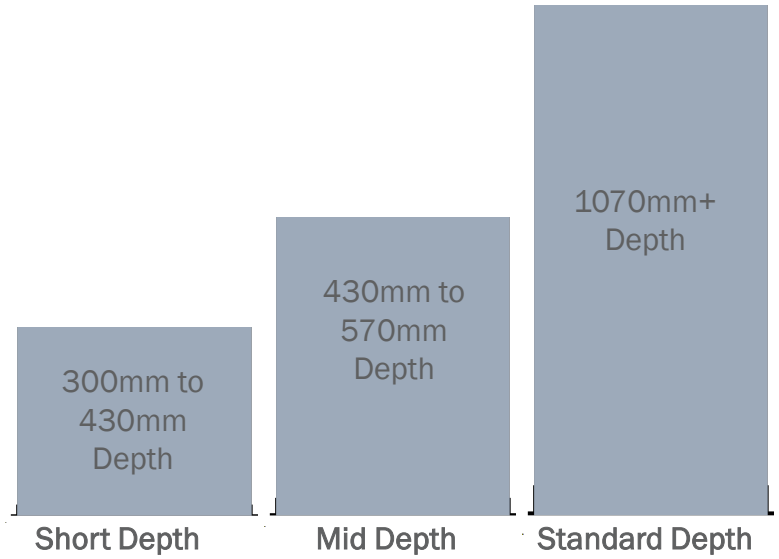


M-DNO Simplified

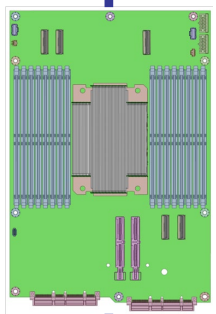
- A family of Partial Width HPMs
- Optimized to 19" and 21" Racks such as Open Rack V3
- Meets the Needs of Form Factor constrained designs
- Specification Scope same as M-FLW
- Generational chassis reuse like M-FLW
- Interface Commonality with M-FLW
- Not chassis compatible with M-FLW
- Platform Customization Zone on Type 4 Only

Targeted Usage of M-DNO Specification

One Basic Architecture

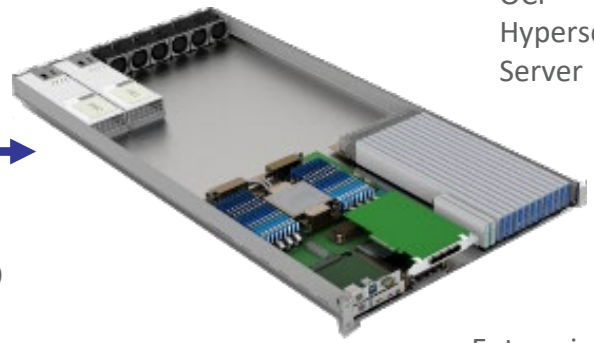


Multiple Product Designs

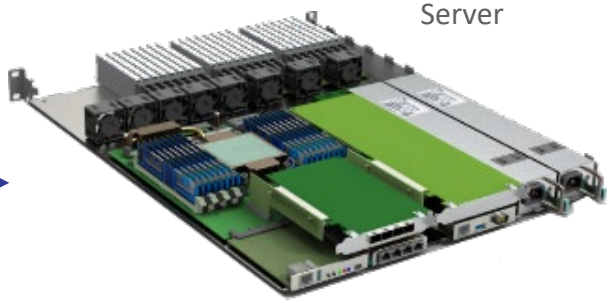


Same M-DNO HPM 3 Different Designs

Short Depth EDGE Server



OCP Hyperscale Server



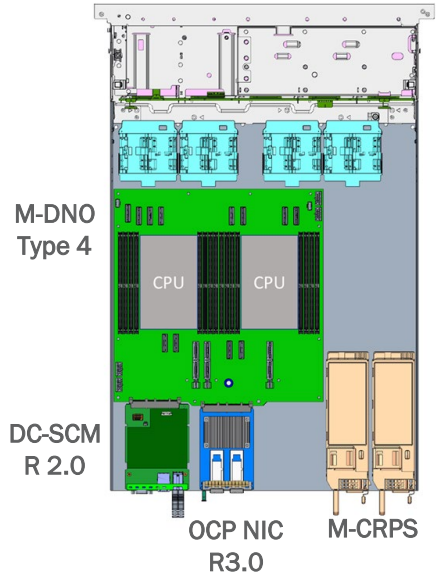
Enterprise Storage Server

- Short / Medium / Standard Depth Racks
- Enterprise, Telco, CSP, Edge….
- Variety of orientations and service models
- Flexible power from front and / or rear side
- HPM supplied power to fixed risers (due to density of systems)

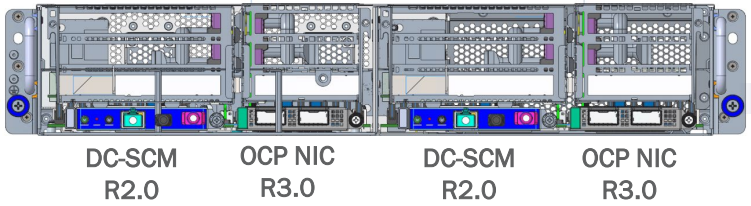
M-DNO “Tenets”

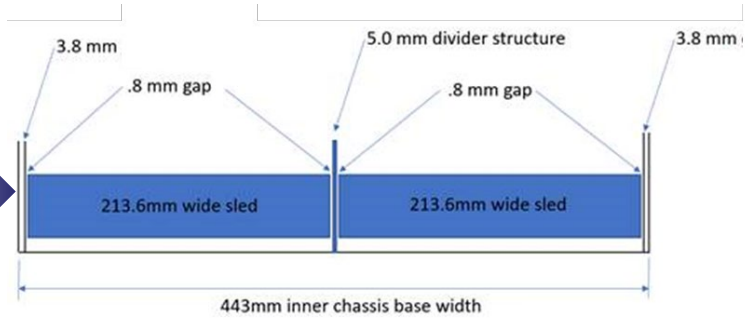
- OCP NIC R3
- OCP DC-SCM R2
- Decoupled Power Supply (PDB or Bus Bar)
- Remote Fans
- Mix of Riser and Cabled I/O (Optional Fixed Connectors)
- ½ Width -> 2 in 19” w/ Static Rails or 21" Open Rack V3
- ¾ Width -> 1 + 2x M-CRPS in 19” w/ Slide Rails or 21" Open Rack V3

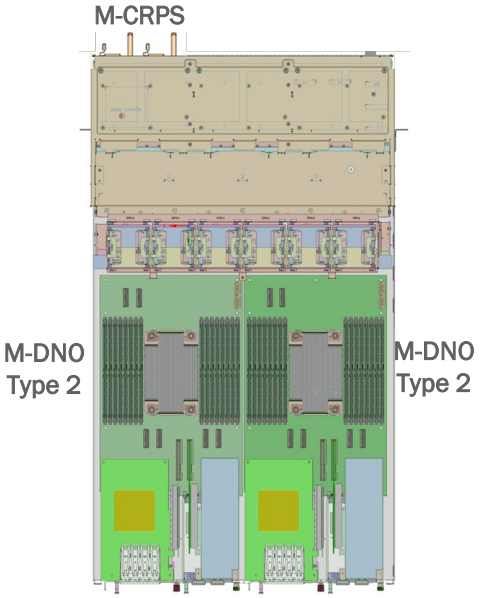
¾ Width Solutions



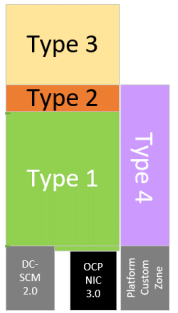
1/2 Width Solutions







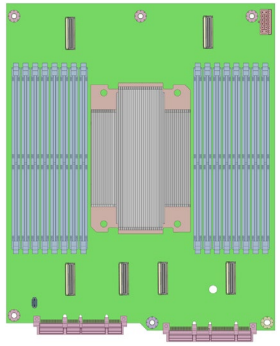
Board Type Overview



Type 1

Depth Optimized ½ Width

210mm W x 250mm L

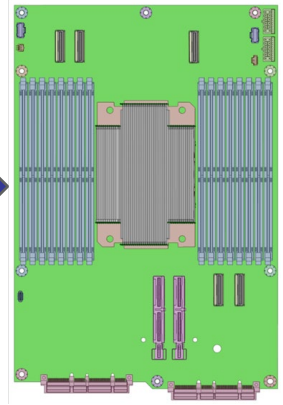


Interop

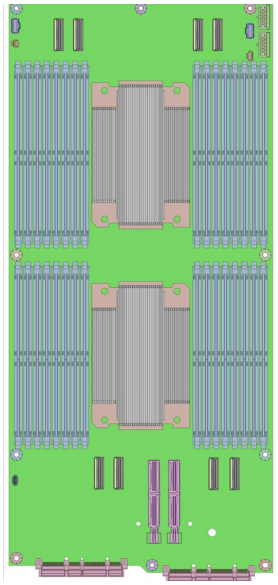
Type 2

Feature Optimized ½ Width

210mm W x 300mm L



Interop

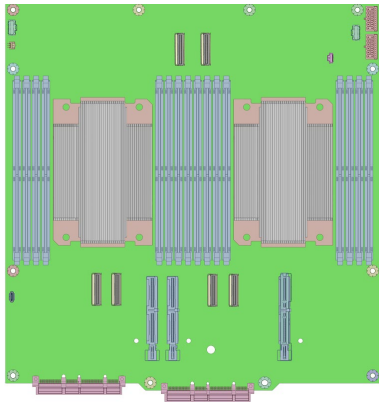


Type 3

Extended Half Width

210mm W x 450mm L

Interop



Type 4

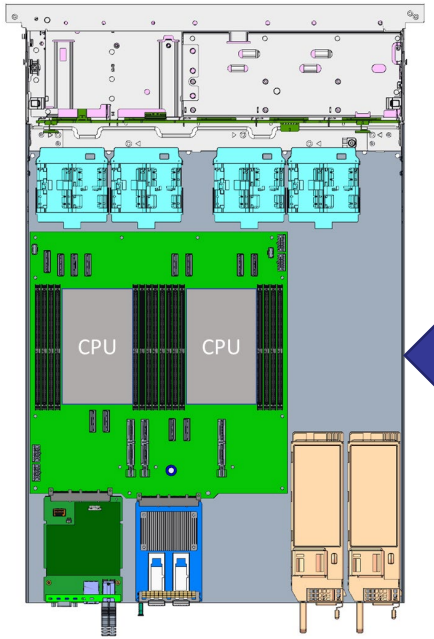
¾ Width

295mm W x 300mm L

Note: HPM Layouts depicted are **EXAMPLES ONLY**, many of the details are not specified by the M-DNO specification (DIMM count, connector locations and quantities, exact CPU placement, etc.)

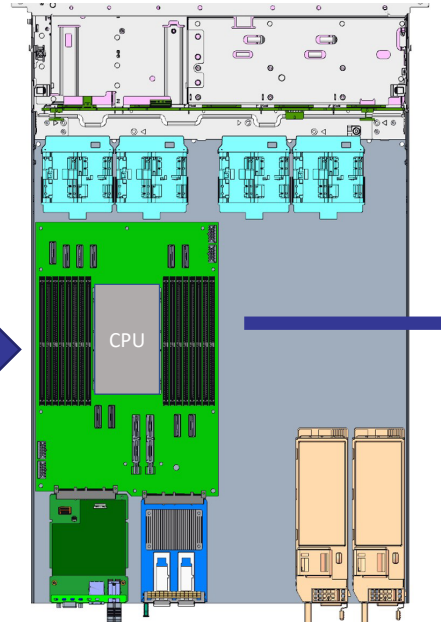
Board Type Interoperability

Type 4 HPM

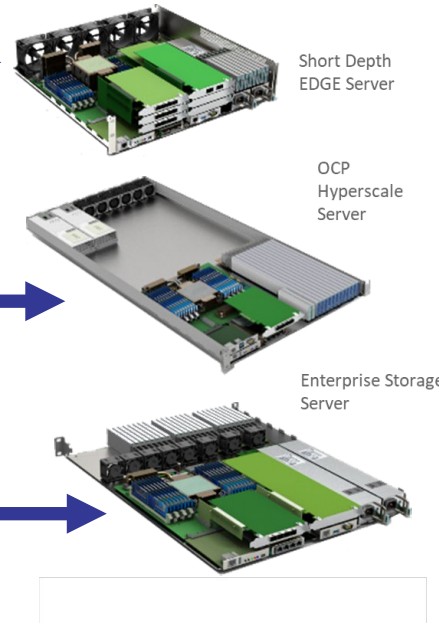


One Chassis Infrastructure
Supports Multiple M-DNO Types

Type 2 HPM

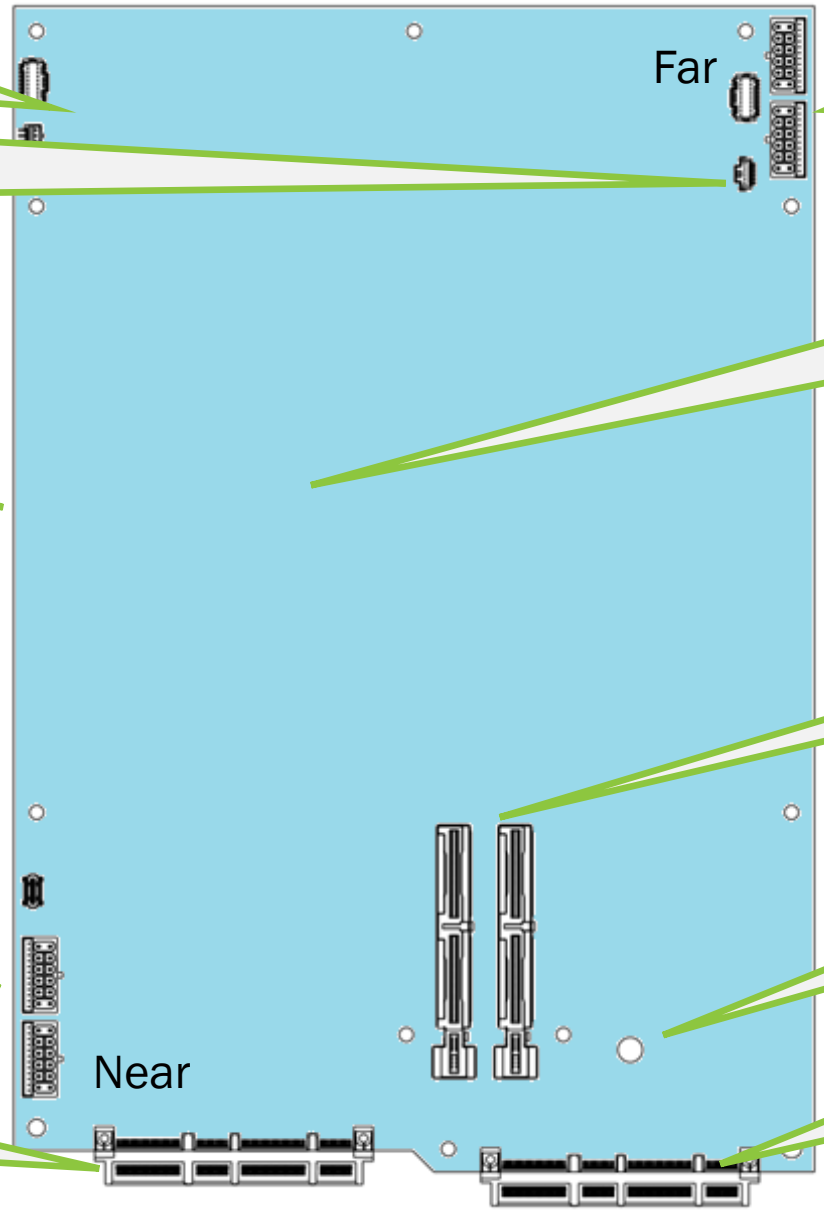


One HPM Enables multiple product designs



- Systems designed for larger M-DNO HPM Types also support smaller Types
- Enabled via careful selection of mounting locations and bottom side keep-outs
- DC-SCM, NIC and I/O Riser locations consistent across all board types

M-DNO Spec Scope Overview



Miscellaneous Headers (Control Panel, USB, etc.) compliant with M-PIC

M-PIC Complaint Ingress / Egress Power Connector(s) Location

Component height restrictions, keep out zones, etc.

Board Type Outlines (4x)

Fixed M-XIO Compliant Riser Locations

M-PIC Complaint Ingress / Egress Power Connector(s) Location

Mounting and Retention Hole Locations

DC-SCM R2.0 Connector Location

OCP NIC R3.0 Connector Location

Contact Us

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- Send feedback or questions to
  - Mike Gregoire, michael.gregoire@dell.com
  - Dirk Blevins, dirk.blevins@intel.com
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Next up

@ 9:25 PDT

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M-PIC	Platform Infrastructure Connectivity
M-XIO	Extensible I/O
M-PESTI	Peripheral Sideband Tunneling Interface
M-CRPS	Common Redundant Power Supply

DC-SCM 2.0

Q&A and Discussion

Platform Infrastructure Connectivity (M-PIC)

as part of the DC-MHS Family

Clifford DuBay

Tim Lambert

The Role of M-PIC R1 in DC-MHS

Define and standardize connectors and interfaces and provide guidance needed to interface HPMs to platform and chassis infrastructure elements and subsystems.

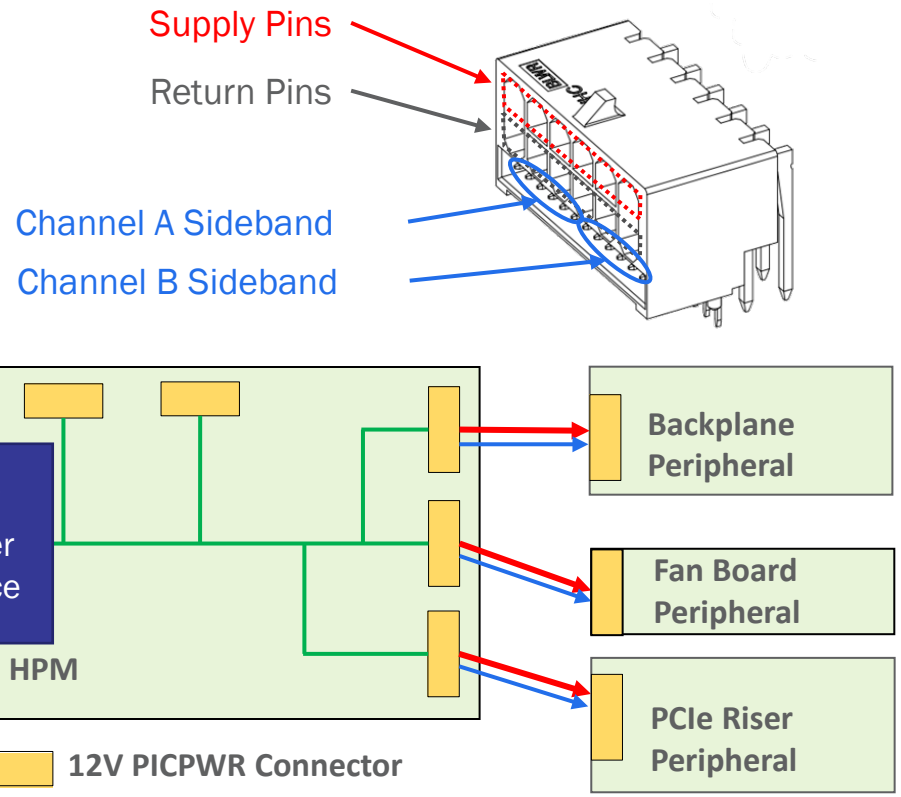
- M-PIC defines connectors and interfaces
- M-PIC defines common connectors
- M-PIC provides interface guidance

Note: M-PIC does not cover Items defined in other OCP or DC-MHS specifications.

M-PIC defined connectors and interfaces

- The 12V Power Architecture Vision:
  - Provides 12V when any PSU output is enabled.
  - Provides flexible sidebands for control and management.
  - Defines 12V PICPWR connectors with 2 channels.
  - Ensures 12V PICPWR is keyed differently than 12VHPWR.
  - Allows for power ingress or egress.
  - Moves power gating from HPM to peripherals.
  - Defines a connector for (PDB to HPM) analog monitoring.
- The 48V Power Architecture Vision:
  - Will add 48V support for Open Rack V3 and 48VHPWR AICs.
  - Will define Topologies and connectors.
  - Feedback on 48V usage is appreciated.

12V PICPWR Example

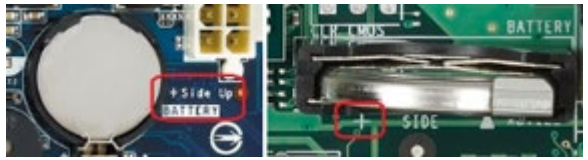


M-PIC defined connectors and interfaces

- The Primary Control Panel Vision:
  - Covers the maximum number of control panel features proposed.
  - Provides flexible sidebands for control and management.
  - Uses 12V power for control panel.
  - Includes a SPI interface.
  - Includes USB2 from DC-SCM.
- The Control Panel Quantity Vision:
  - Provides control panel flexibility by defining a 2nd connector.
  - Ensures control panel pinouts are electrically safe.

Common Connectors

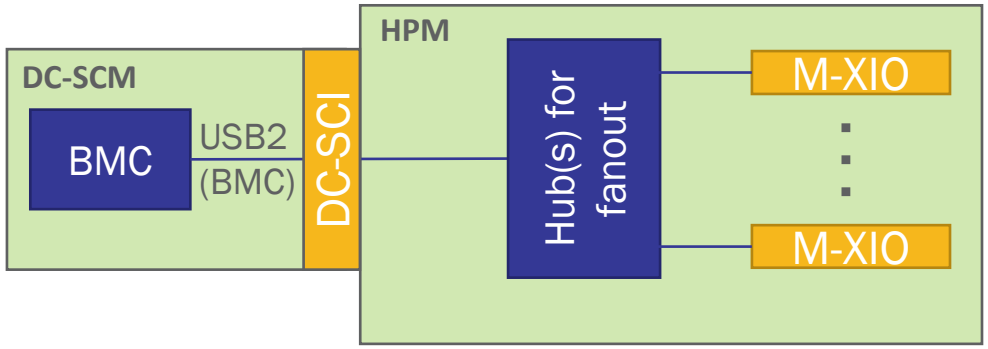
- M-PIC defines common connectors
  - Intrusion Switch Header - M-PIC defines a 3-pin positive latching header with a cable presence.
  - Internal USB3 Host connector – M-PIC specifies a USB3.1 vertical Type C connector.
    - M-PIC welcomes feedback regarding Type A vs Type C and usage cases (e.g., debug vs a product requirement).
  - Coin Cell Battery Holder – M-PIC defines the RTC battery holder sized for CR2032.



Interface guidance

- Cabled Boot Storage Peripheral (optional) is enabled by adoption of M-XIO x4 and a 12V PICPWR connection.
- DC-SCM Revision 2.0 is adopted for its improved features and for OCP alignment.
- Smart NIC Management Connectivity

  M-PIC supports the option to interface using BMC USB2.0 host signals from HPM through M-XIO to peripherals (x8 cable or wider).



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M-CRPS	Common Redundant Power Supply

DC-SCM 2.0

Q&A and Discussion

Modular – eXtensible I/O (M-XIO)

as part of the DC-MHS Family

Javier Lasa

Charles Ziegler

M-XIO Introduction

Goals:

- Aligns with PCI-SIG Cable/Connector Gen 5/6 WIP specification.
- Contains a minimalist set of sideband signals to accommodate SFF-TA-1016 (PCI-SIG Connector Choice).
- Support for both cabled and PCB risers.
- Optional support for M-PESTI FW upgrade to accommodate new peripheral modules without adding physical signals or pins.

M-XIO Does:

- Define a minimal set of requirements for a connector to be M-XIO compliant.
- Enable connectivity to EDSFF, Raid Controllers, PCIe CEM compliant cards and OCP NIC 3.0 devices through the use of intermediary-boards (ex. a paddle card) with remote circuitry.
- Define pinouts of signals for choice connectors (to date: SFF-TA-1016, SFF-TA-1026, and Multi-Track).

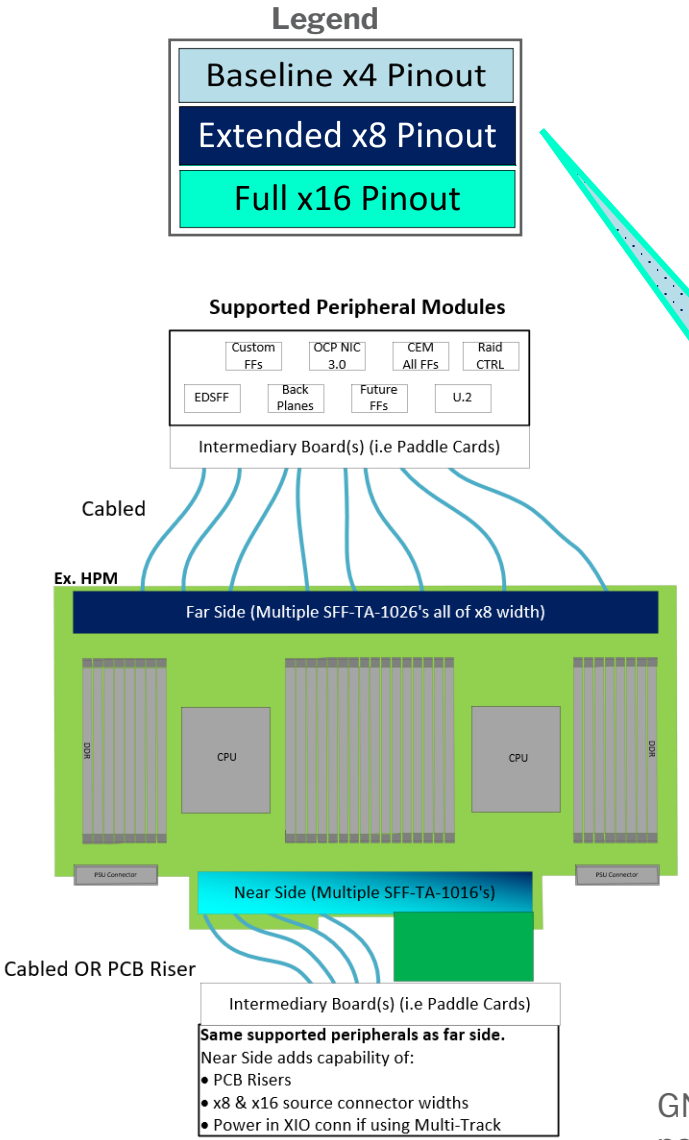
M-XIO Does not:

- Require specific connector, it is meant to be used across multiple generations of products and connectors.

M-XIO (Modular – eXtensible IO)

M-XIO refers to HPM High-Speed PCIE and Peripheral Sideband connectivity

Goal: Support Interchangeable peripheral HW off HPMs



Create a Universal HSIO Signal List:

x4
PCIE x4
SMBUS (2)
PERST_N (1)
CBL_PRES_PESTI_N (1)
FLEXIO (1)
3p3AUX_MGMT (1)
REFCLK (2)

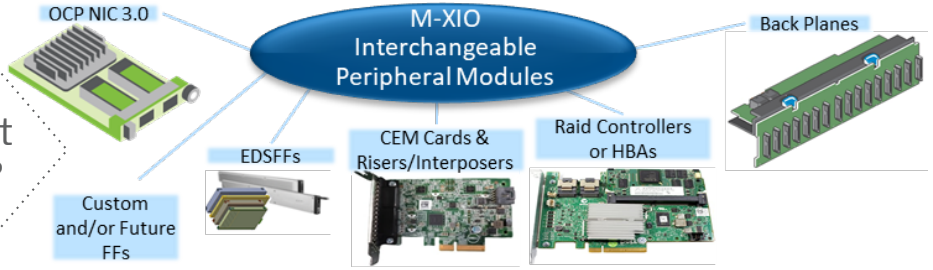
x8 adders
PCIE x4
USB 2.0 (2)
FLEXIO (6)

x16 adders
PCIE x8
Optional:
Duplicate x8 SB (16)
PICPWR Section (12)

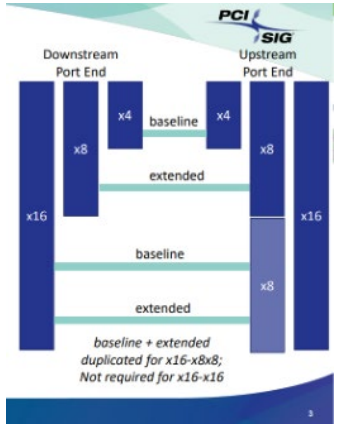
GNDs distributed throughout for isolation and return paths

How to enable via M-XIO?

What HW?



Align w/ PCI-SIG

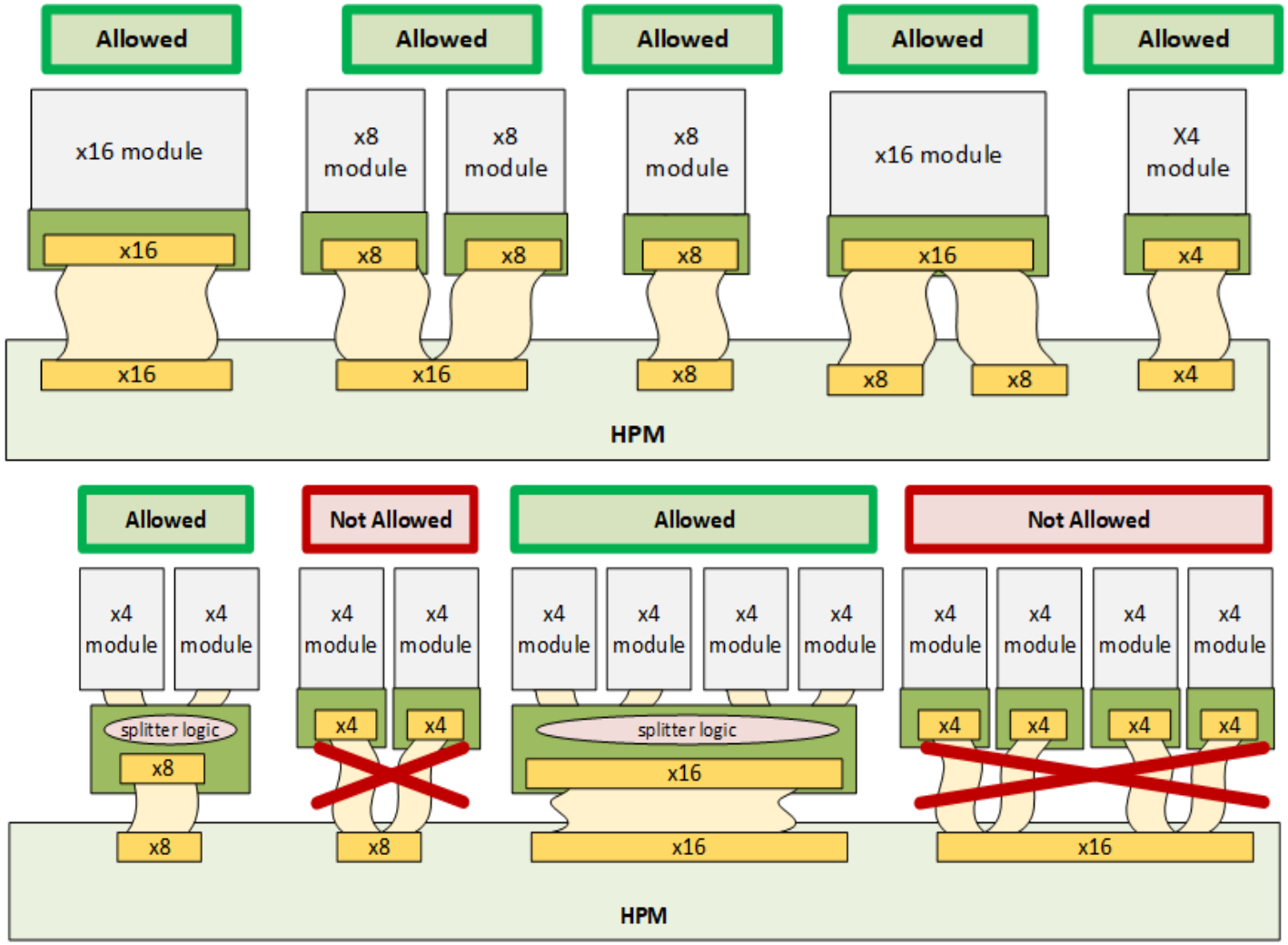


https://members.pcisig.com/wg/PCI-SIG-WG_Members/document/16930

DC-MHS M-XIO Output: Universal Signal List & Pinouts
M-XIO v0.7 Specification

Connect. Collaborate. Accelerate.

M-XIO Connector Width & Cable Options



*The above figure is meant to depict common configurations; it is not an exhaustive list of all possible and not possible combinations.

- Even though any combination of link subdivisions are possible, the only physical cable split allowed is a x16 source to x8x8 at different PCB destinations OR x8x8 sources that combine to a x16 destination.
- The splitter logic depicted is indicative of necessary fanout circuits with optional selective remote and autonomous local controls. This is typically but not limited to PERST, clock and device presence fan out / fan in, etc.

Connect. Collaborate. Accelerate.

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  - Editors: charlie.ziegler@dell.com & javier.lasa@intel.com
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@ 10:10 PDT

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M-CRPS	Common Redundant Power Supply

DC-SCM 2.0

Q&A and Discussion

Modular-PEripheral Sideband Tunneling Interface (M-PESTI)

as part of DC-MHS Family

Overview April 27, 2022 OCP Tech Talk

Tim Lambert

Javier Lasa

DC-MHS Sideband Management

DC-MHS Tenets

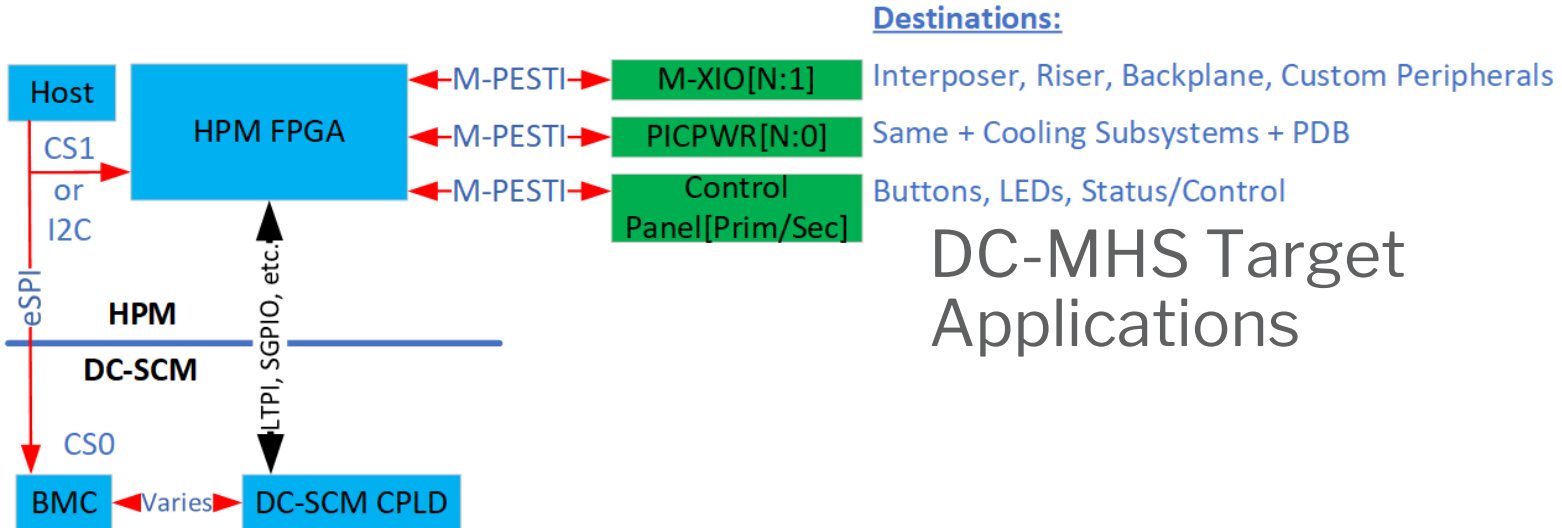
- HPM & Peripheral HW compatibility with maximum leverage/re-use
- Implement flexible and extensible base plumbing
- Plug-n-recode in Phase 1. Plug-n-play comes later.

Systems Management preferred interface order (Generally Accepted)

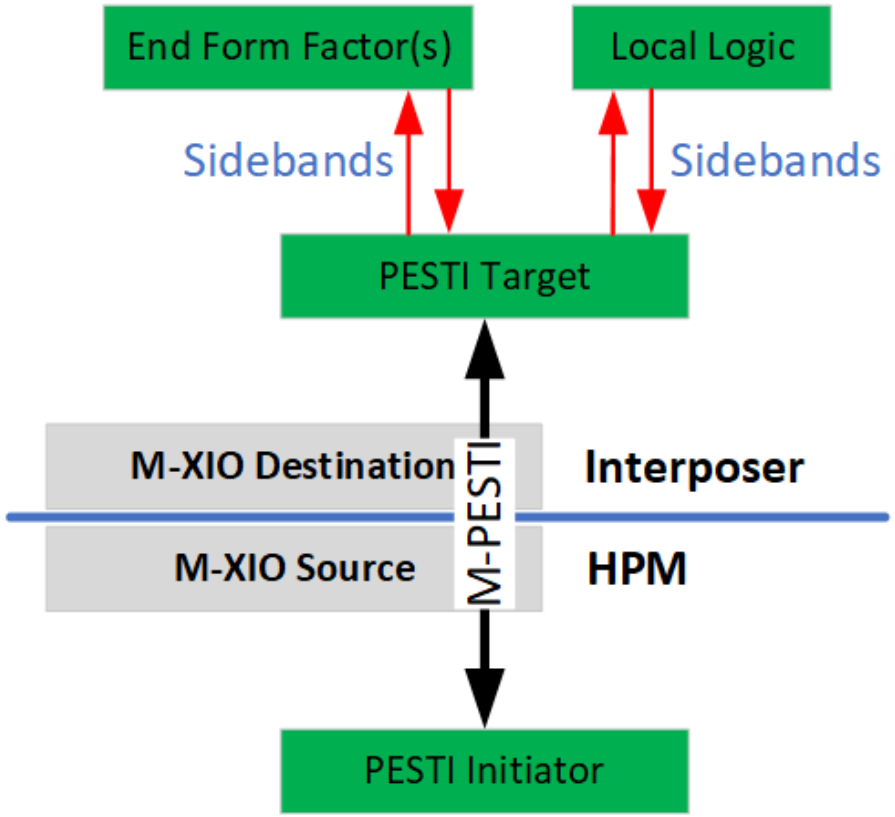
- 1) In-band where possible
- 2) Out-of-band
  - A) **Non-real time** -USB2.0 High Speed, SMBUS/I3C, PCIe VDM (higher level protocols where possible)
  - B) **SW-Defined Real-Time Virtual Wires (M-PESTI)**
    - Robust discoverability
    - Diverse portability of applications - sideband scaling is a very general problem
    - Scalable & Extensible toward high fanout, complex or custom applications
    - FW & Transistors are cheaper and remotely fixable versus real pins & wires
    - Enhanced security
    - Intel's Enhanced SPI is a prior success story (but ~7 wires)
  - C) **Discrete wires**
    - *Never enough* - for legacy & the unknown; M-XIO's Flex I/O count is small
    - *Never wired right* driving HW incompatibilities & heterogeneous M-XIOs

M-PESTI Overview

- Real-time sideband virtualization & self-describing peripheral attributes
  - Ex: PWRBRK, NVMe Hotplug, blink LEDs; MUXSELs, card ID; physical routing topology
- Optional protocol over present wire (no added pin tax)
- 3.3V, 1 wire, half-duplex UART (ubiquitous & simple/low logic)
- Discovery Phase (from present only to full Plug-n-Play)
- Full interconnect source/destination ID
- Real-time Virtual Wire in the Active Phase
- Error Detection; Broadcast support
- Coming Soon: Fanout, Attestation



DC-MHS Target Applications



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DC-SCM 2.0

Q&A and Discussion

Modular Hardware System - Common Redundant Power Supply (M-CRPS)

as part of DC-MHS Family

Aurelio Rodriguez-Echevarria – Jon Lewis

Agenda

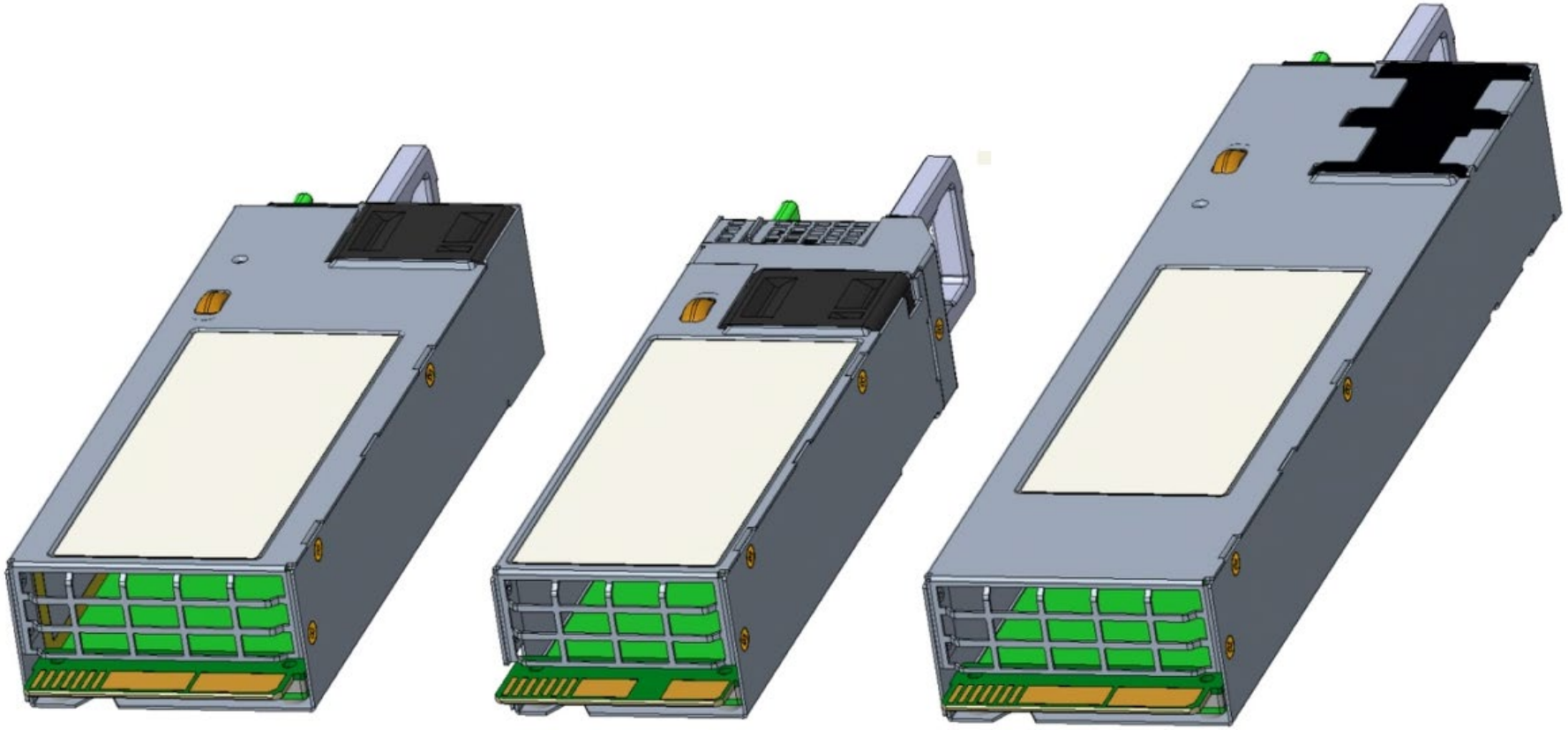
1. Overview
2. Form Factors
3. Hardware features
4. Firmware features
5. Label, handle and latch
6. Configuration file
7. Data & Sidebands Serialization Interface (DSSI)

M-CRPS Overview

The M-CRPS as part of the DC-MHS project addresses the standardization of the server internal redundant power supply specification using the Legacy CRPS as a starting point and creating an evolution with new features that will be useful for all the customers, this way the power supply vendors can focus on designing and develop products based on a standardized specification leveraging the same form factors and Firmware base codes for new products and applying different specifications depending on the end market e.g. Enterprise, Telecom, Cloud, etc.

New features for higher flexibility includes configurability for : LED behavior, Fault and Warning thresholds and more. The M-CRPS introduces a deterministic serialization interface to facilitate the addition of more signals without changing the output connector. Also includes a customizable label artwork and latch finger grip color/design.

M-CRPS Form Factors



185mm by 73.5mm

185mm by 60mm

265mm by 73.5mm

- 185mm by 60mm can be installed in a 185mm by 73.5mm bay with fillers at the sides

Connect. Collaborate. Accelerate.

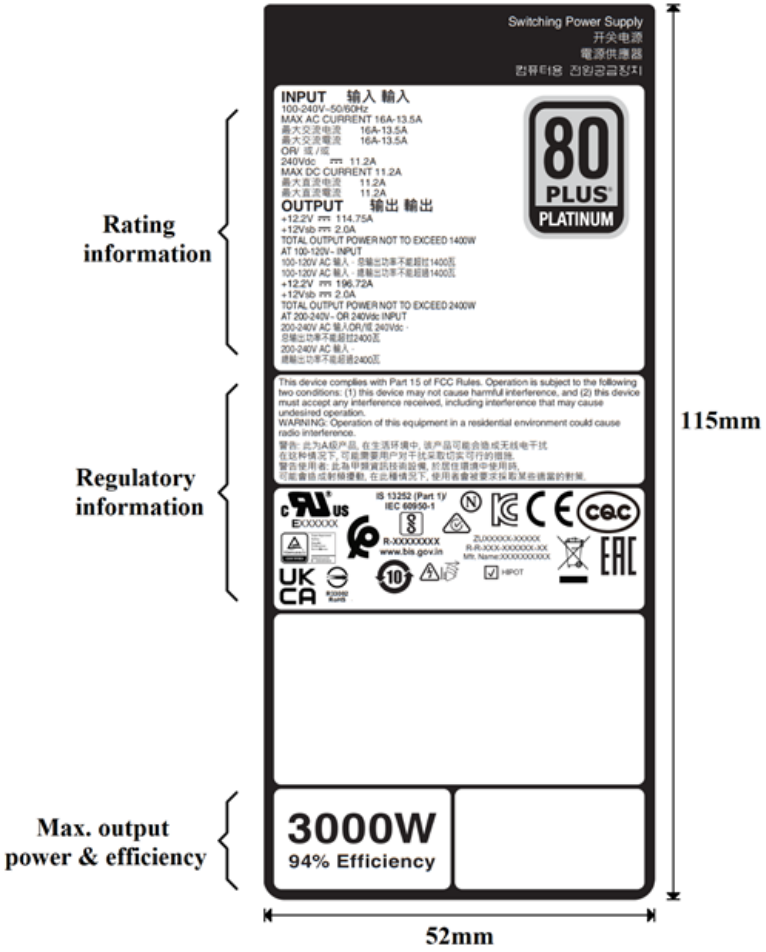
M-CRPS Hardware Features

- PL1, PL2, PL3 and PL4 capabilities.
- Multiple input types: 240VAC/VDC, 277VAC, 380VDC, +54VDC or -48VDC.
- Current sharing mechanism for the main output capable of supporting different vendors in the same system. Up to 6 PSUs in parallel.
- Current sharing mechanism in auxiliary output.
- Imon: current monitoring capability.
- 1-wire Data & Sidebands Serialization Interface (DSSI) for GPIO expansion.
- Illuminated handle for ease of in-rack PSU status identification.
- Common output interface.
- Available customizations for: Label artwork, latch plastic grip design & color.
- Acoustics and Vibration profiles for different environments like: Enterprise, Home/Office and High-Performance Computing.
- Backwards compatible with the Legacy CRPS

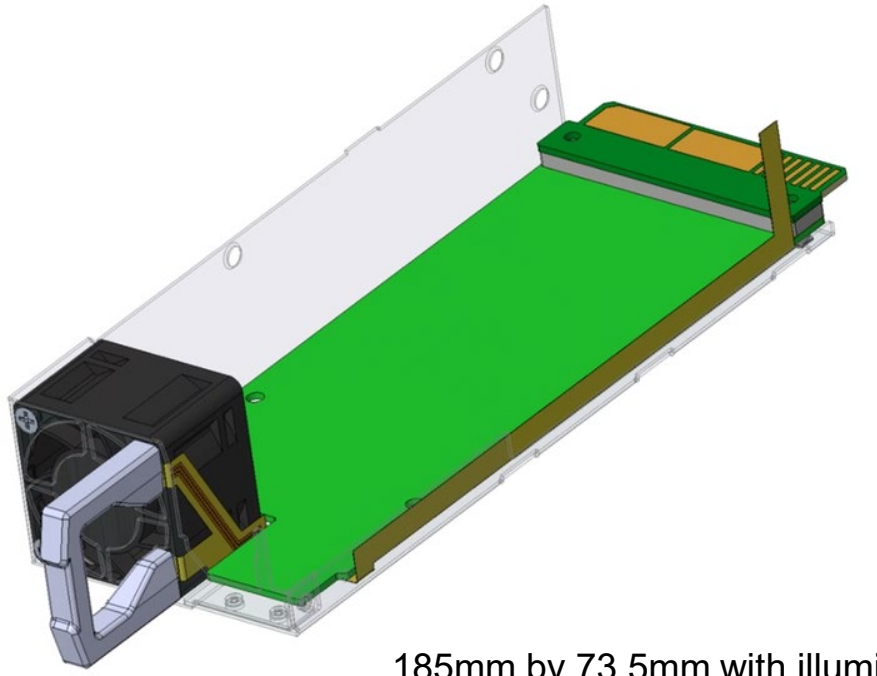
M-CRPS Firmware Features

- Configuration file to customize behavioral aspects like:
  - LED blinking pattern .
  - Latch on fault or retry.
  - Timing characteristics.
  - Fault and warning behaviors.
  - Ability to execute custom pieces of code.
- In-field Firmware upgrade.
- Signed Firmware image and secure Firmware update.
- Blackbox to log fault conditions.
- SMBus communication up to 400KHz.
- Up to 6 SMBus addresses using a single pin (backwards compatible with 2-pin addressing).
- Default fan speed control algorithm based on PID control
- And more.

M-CRPS Label, handle and latch



Label artwork



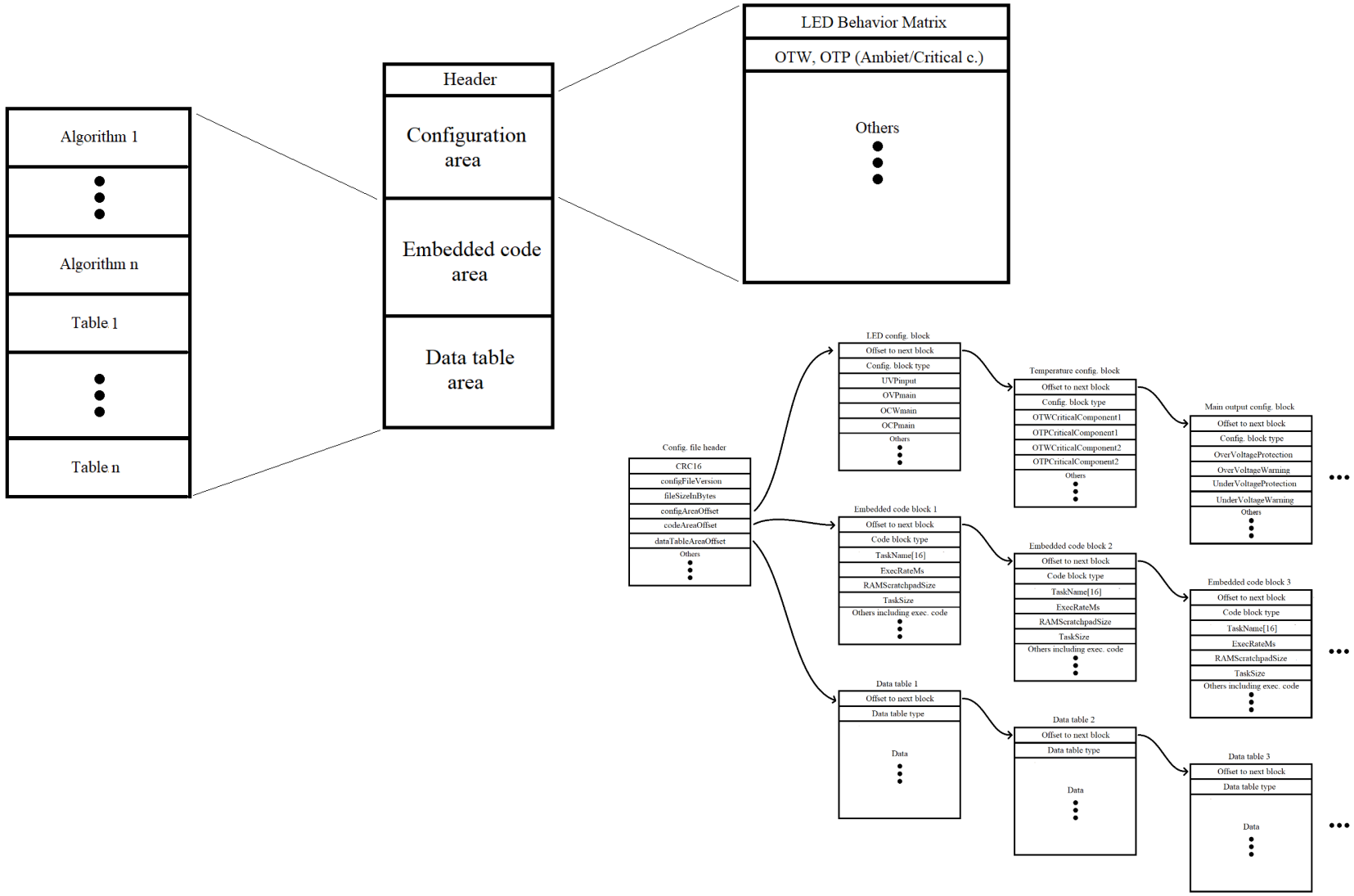
185mm by 73.5mm with illuminated handle using a flex PCB

Plastic finger grip options

- Flex PCB could be used to route fan power and signals

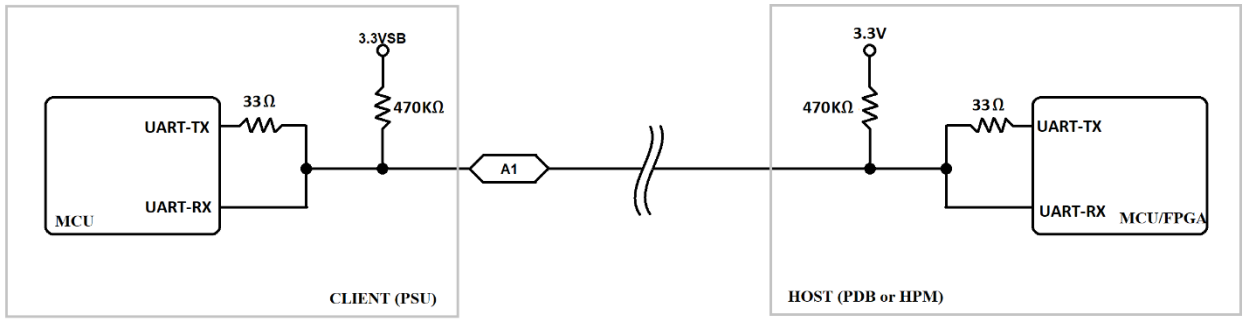
Connect. Collaborate. Accelerate.

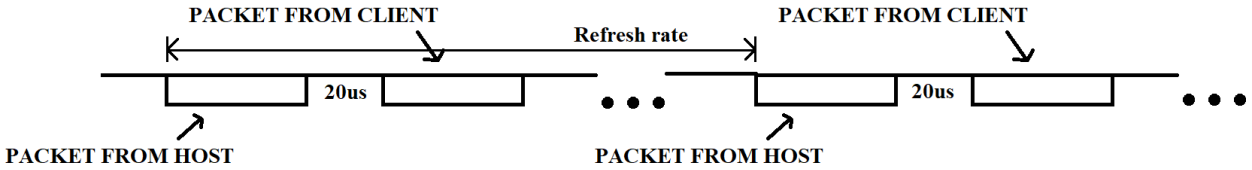
M-CRPS Configuration File



- Main goal is to provide flexibility

M-CRPS Data & Sidebands Serialization Interface (DSSI)





- Main goal is to avoid higher pin count for side band signals in the output connector

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@ 10:40 PDT

DC-SCM 2.0

Q&A and Discussion